

# Compal Confidential

## QAL51 MB Schematic Document

### LA-7871P

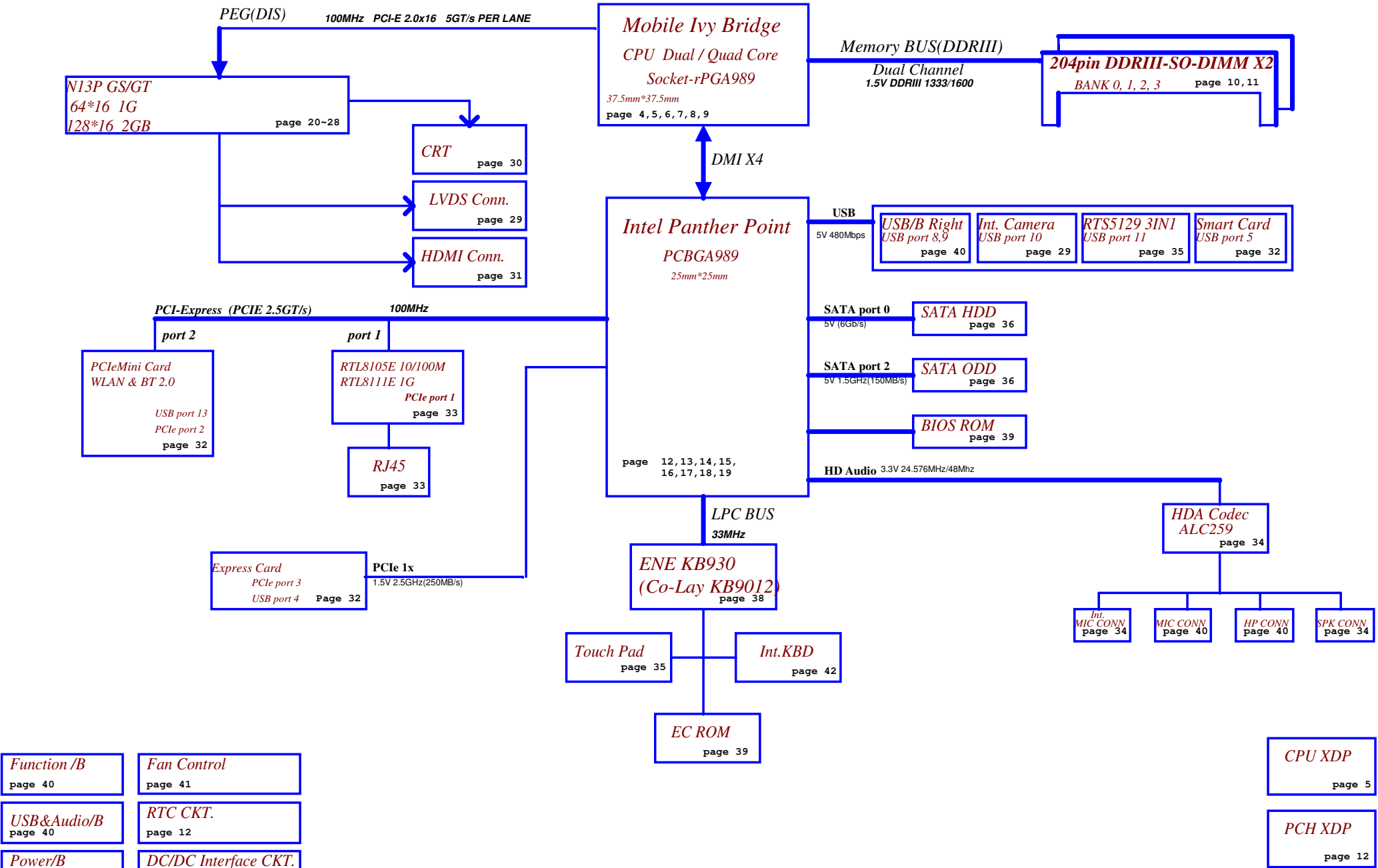
Intel Ivy Bridge / Panther Point

Discrete : N13P-GS / N13P-GT

Rev: 1.0

2012.02.29

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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	QAL30
1	QAL31 / LP
2	QAL31 / GT
3	
4	QAL50
5	QAL51 / GS
6	
7	QAL51 / GT

PCH

USB PORT#	DESTINATION
0	USB2/3 (Left Hand side front)
1	USB2/3 (Left Hand side back)
2	None
3	None
4	USB2 (Right Hand side front)
5	Smart CARD
6	None
7	None
8	EXPRESS CARD
9	USB2 (Right Hand side back)
10	CAMERA
11	Card Reader
12	Finger Print
13	BT Comb

SMBUS Control Table

	SOURCE	MIINI1	BATT 0001 011x b	SODIMM 1001 000x b	SODIMM 1001 010x b	VGA Int. Thermal 0x9A	JXDP1 JXDP2
EC_SMB_CK1 EC_SMB_DA1	KB930 KB9012	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930 KB9012	X	X	X	X	V	X
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V	X	V
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	X	V	X

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	TPM
PCI3	None
PCI4	None

OPTIMUS: XDP@/D@

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	Express Card	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	VGA		
	CLKOUT_PEG_B	None		

Symbol Note :

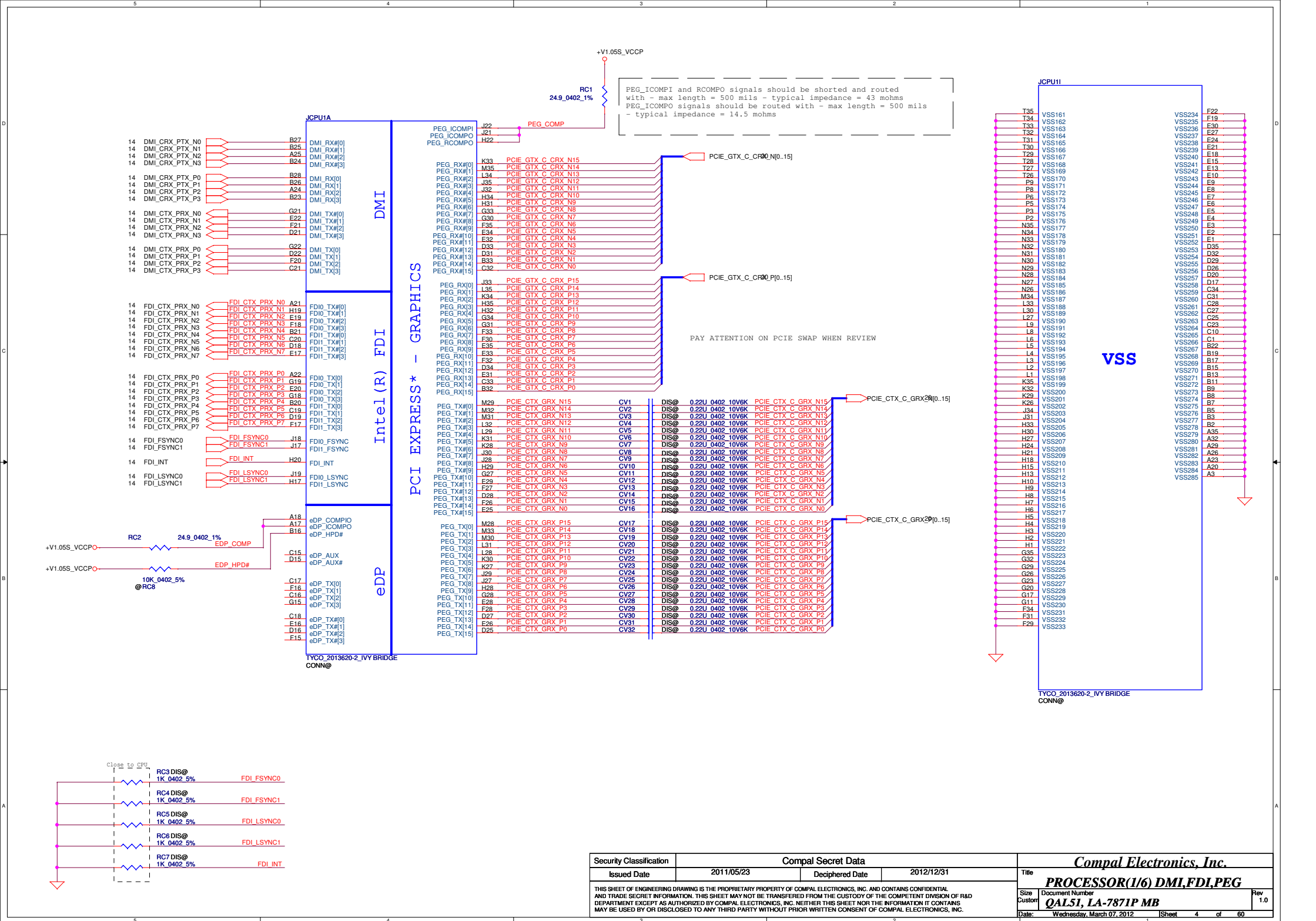
 : means Digital Ground

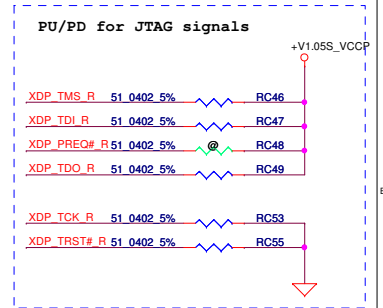
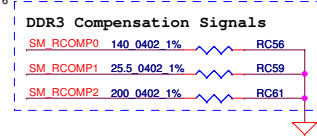
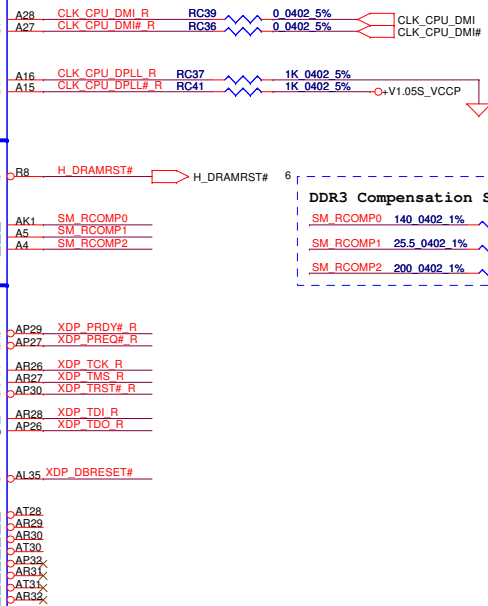
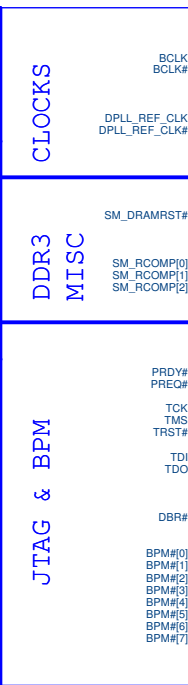
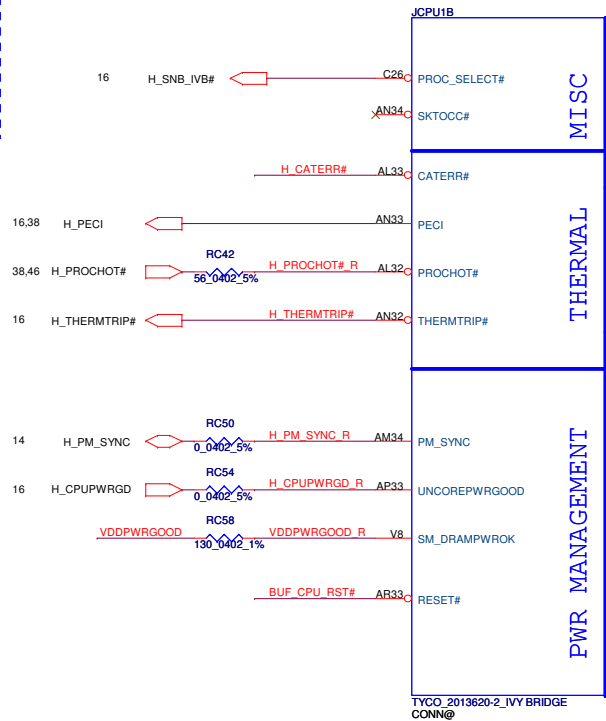
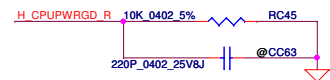
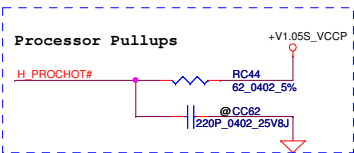
 : means Analog Ground

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	LAN
Lane 2	WLAN
Lane 3	Express Card
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

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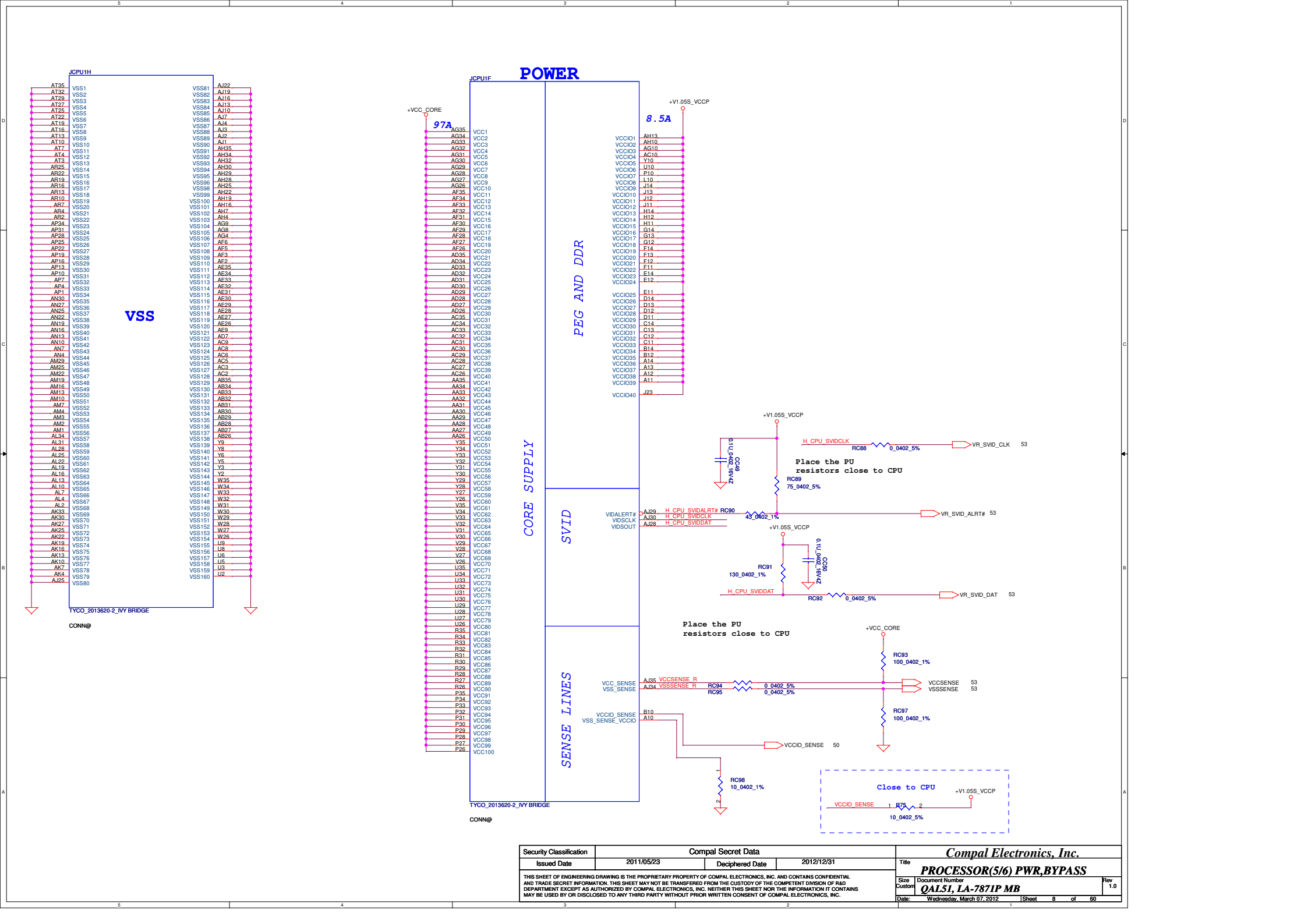


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Deciphered Date				2012/12/31				PROCESSOR(2/6) PM,XDP,CLK			
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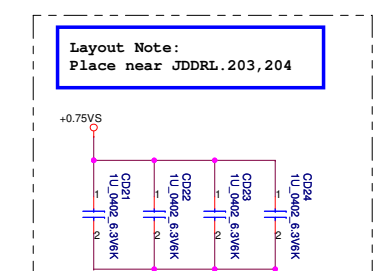
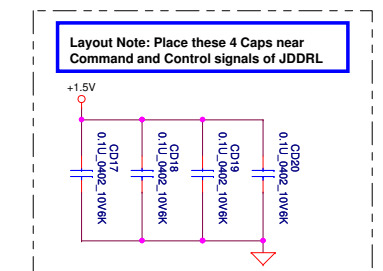
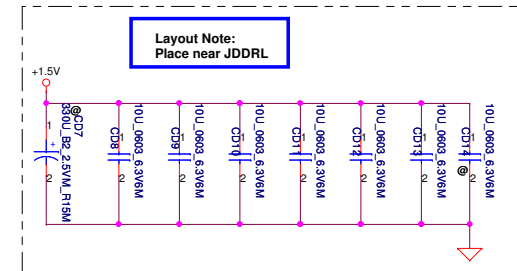
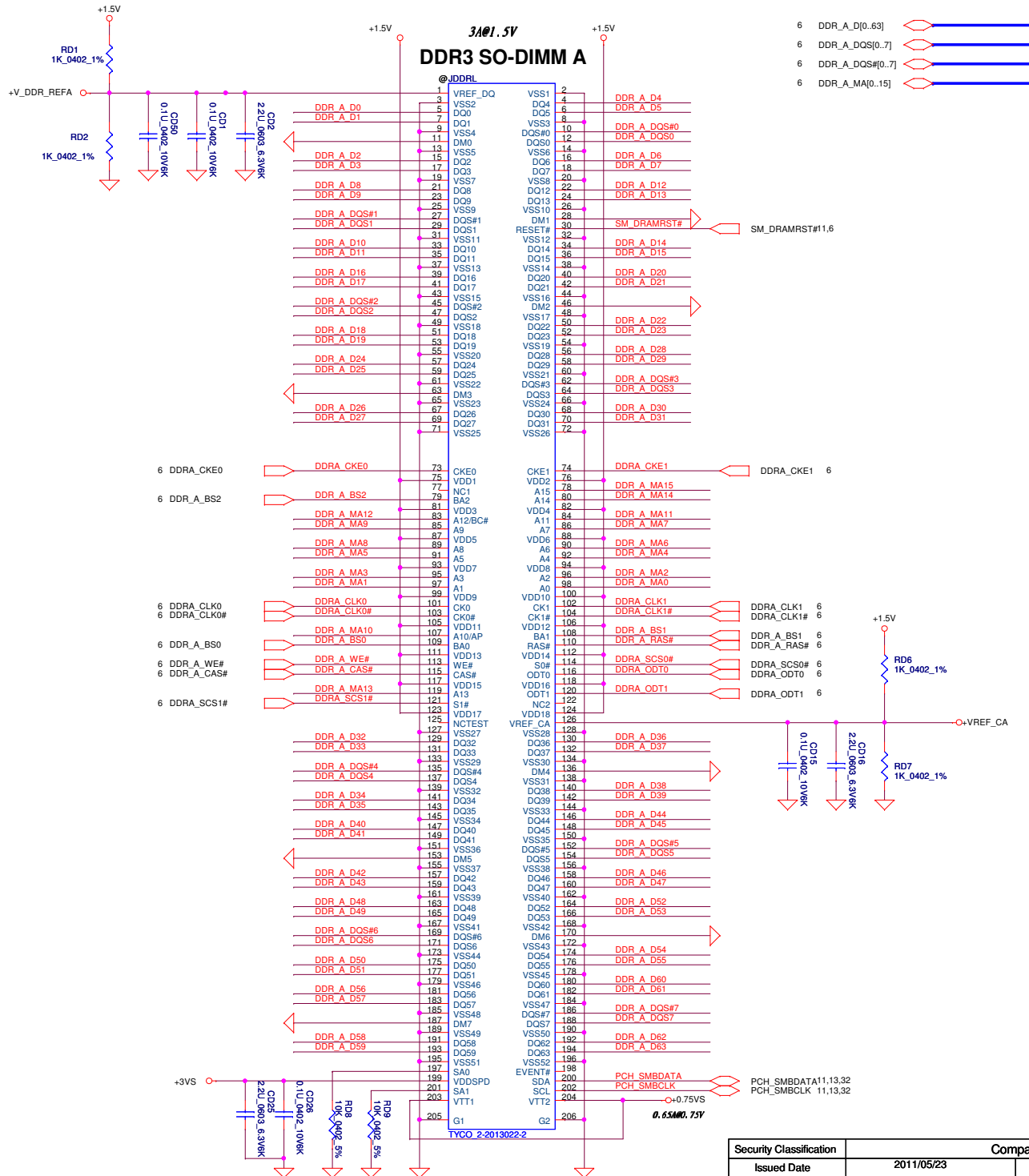




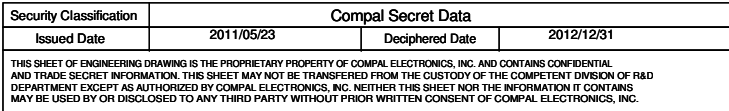


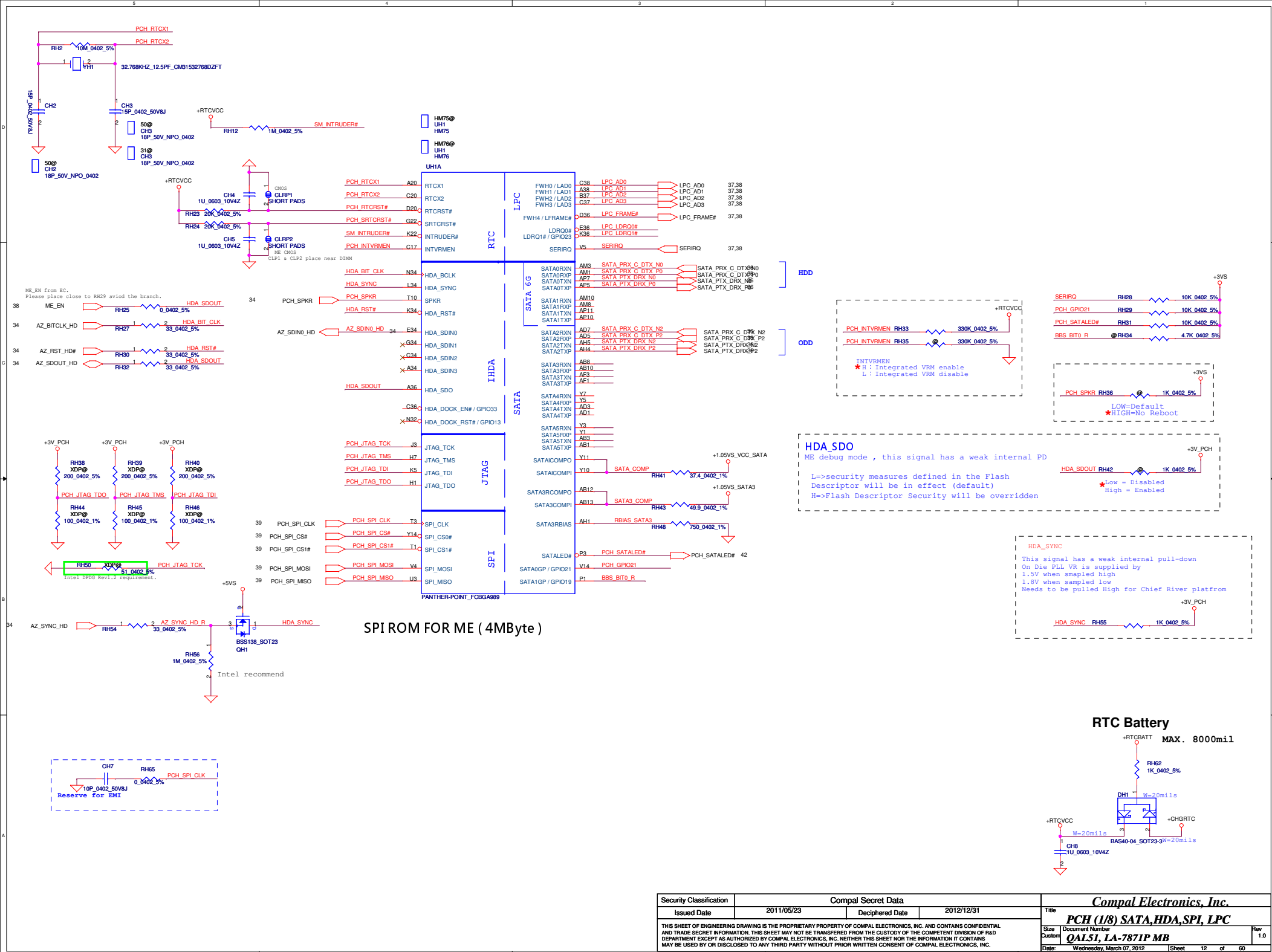




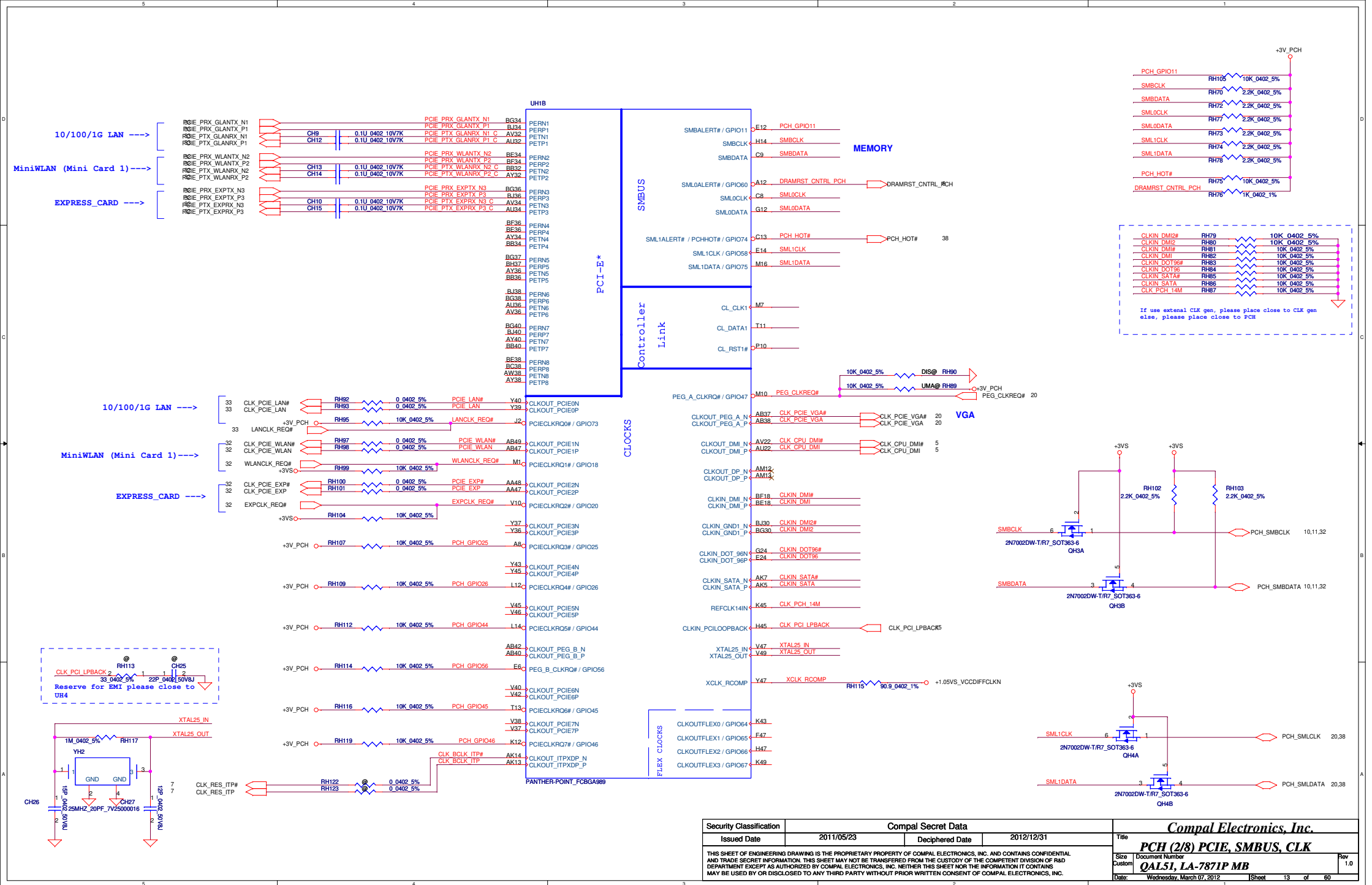


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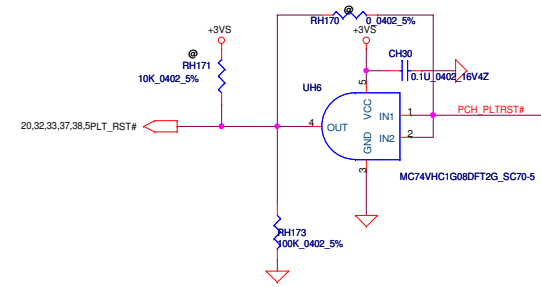
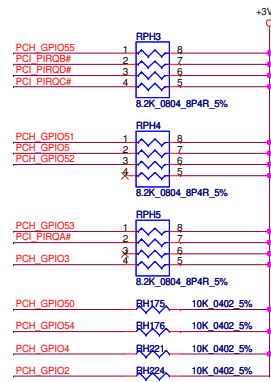
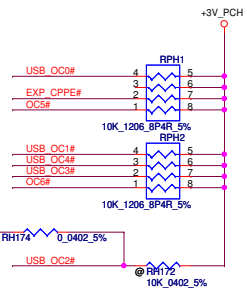
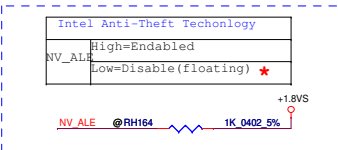
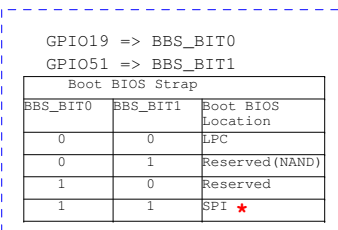
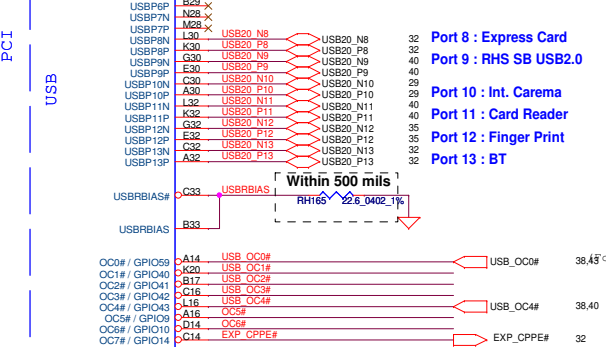
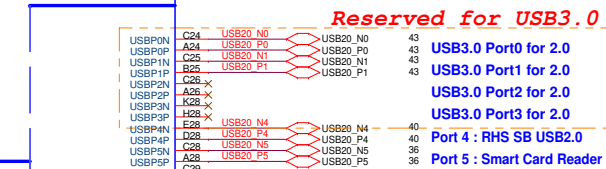
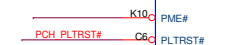
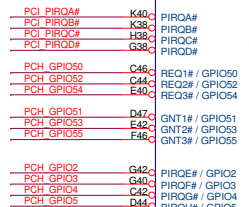


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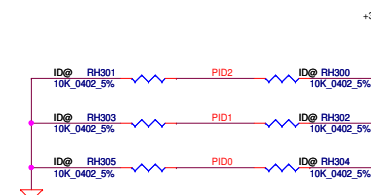
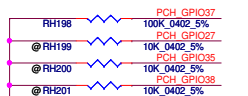
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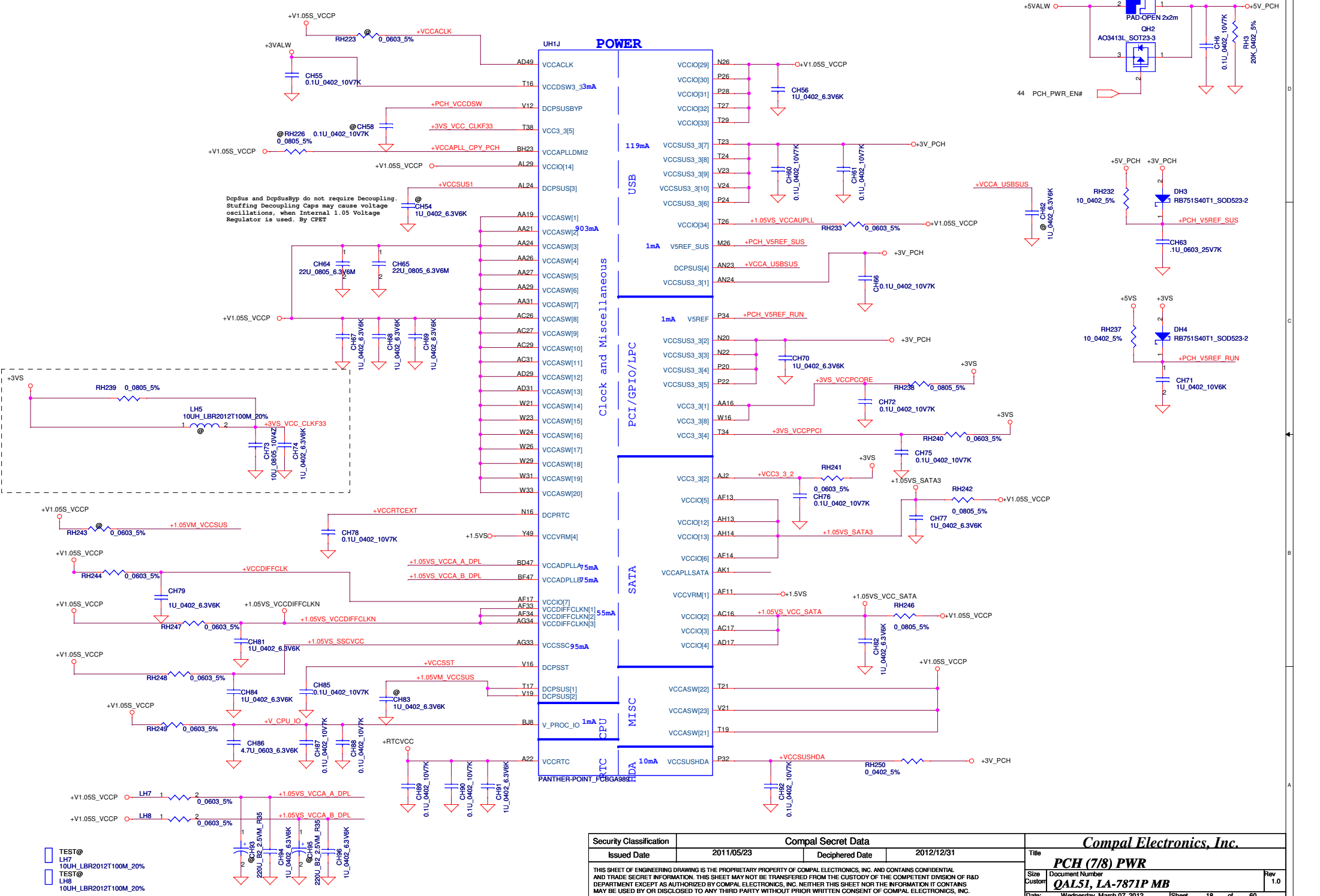
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Please refer to Huron River Debug Board DG 1.2

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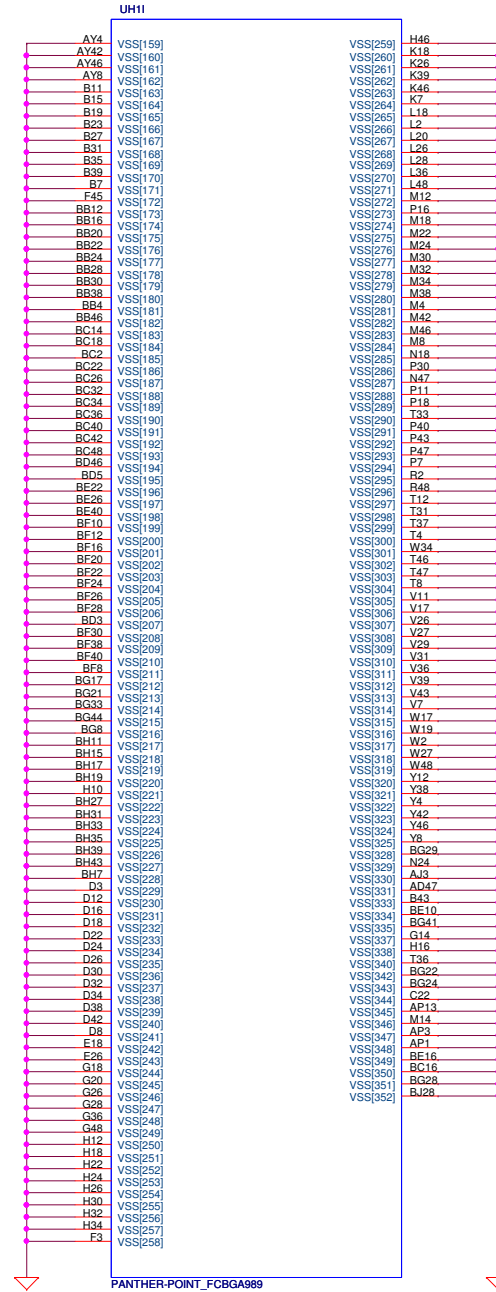
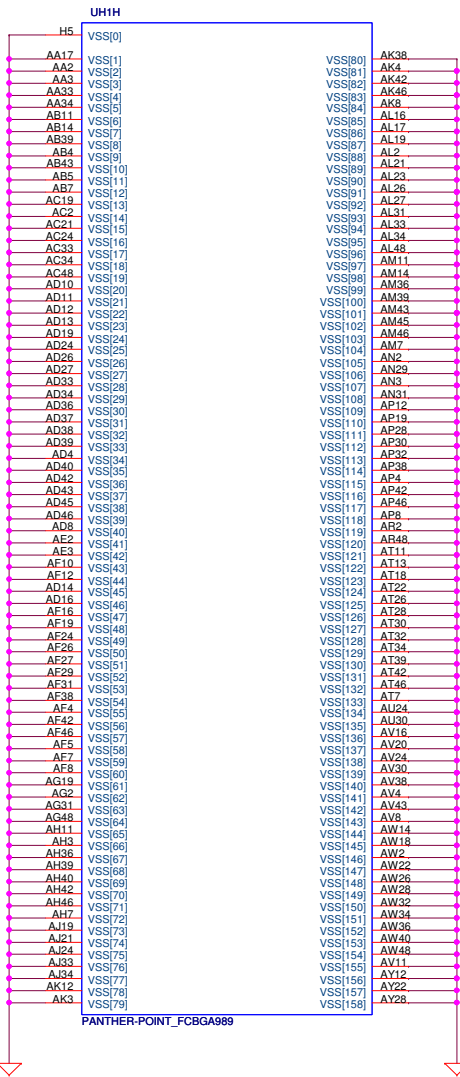




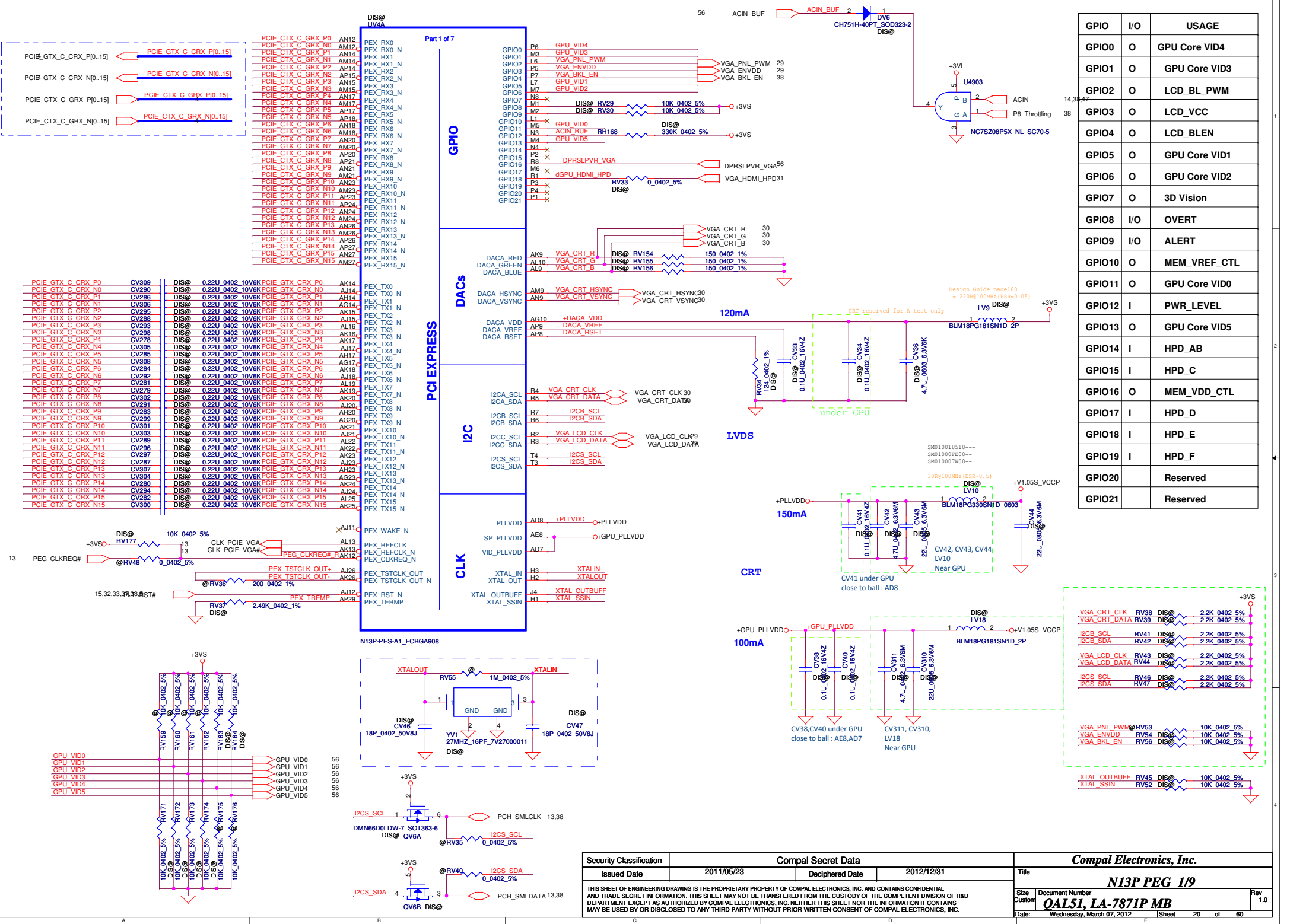


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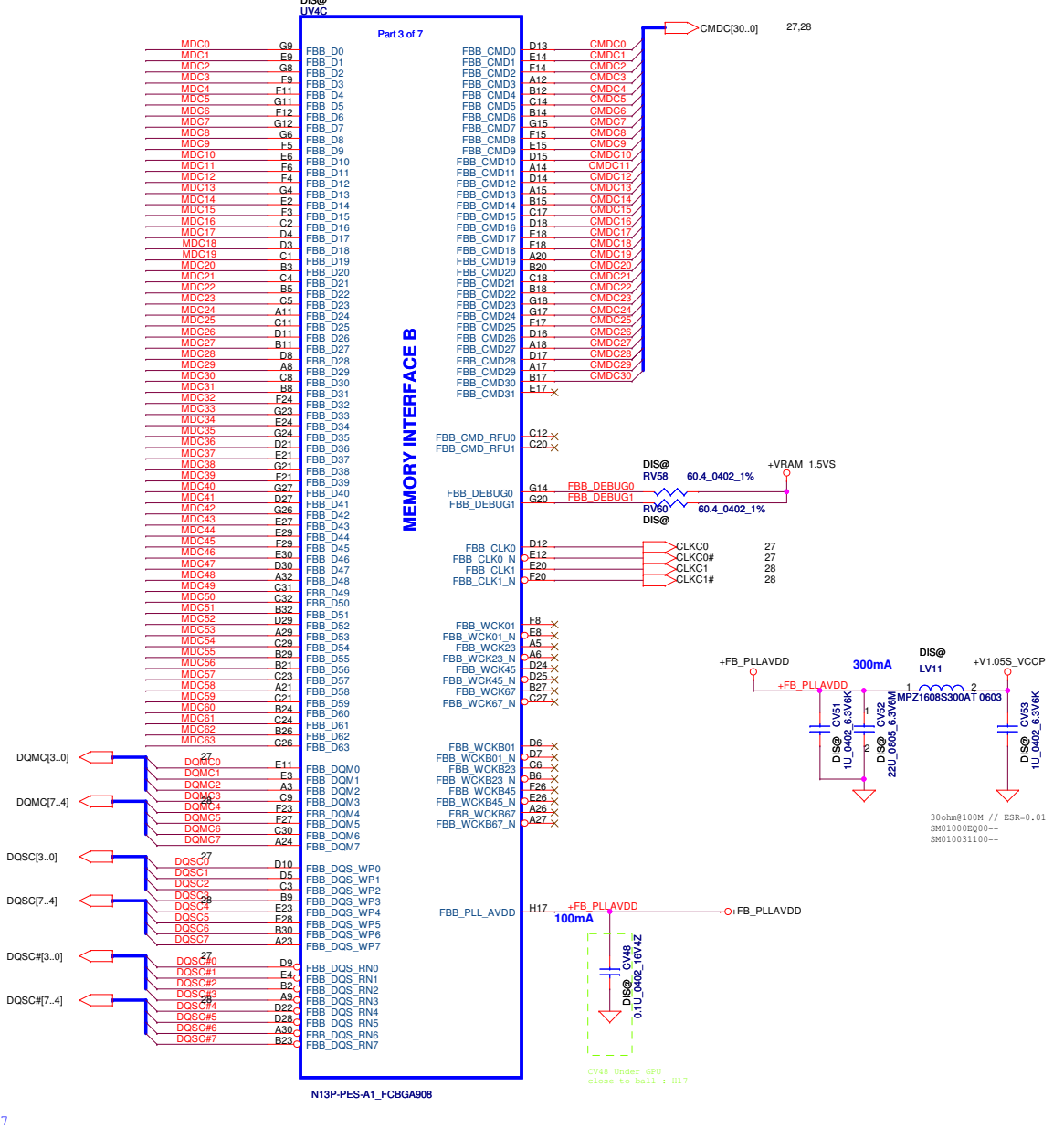
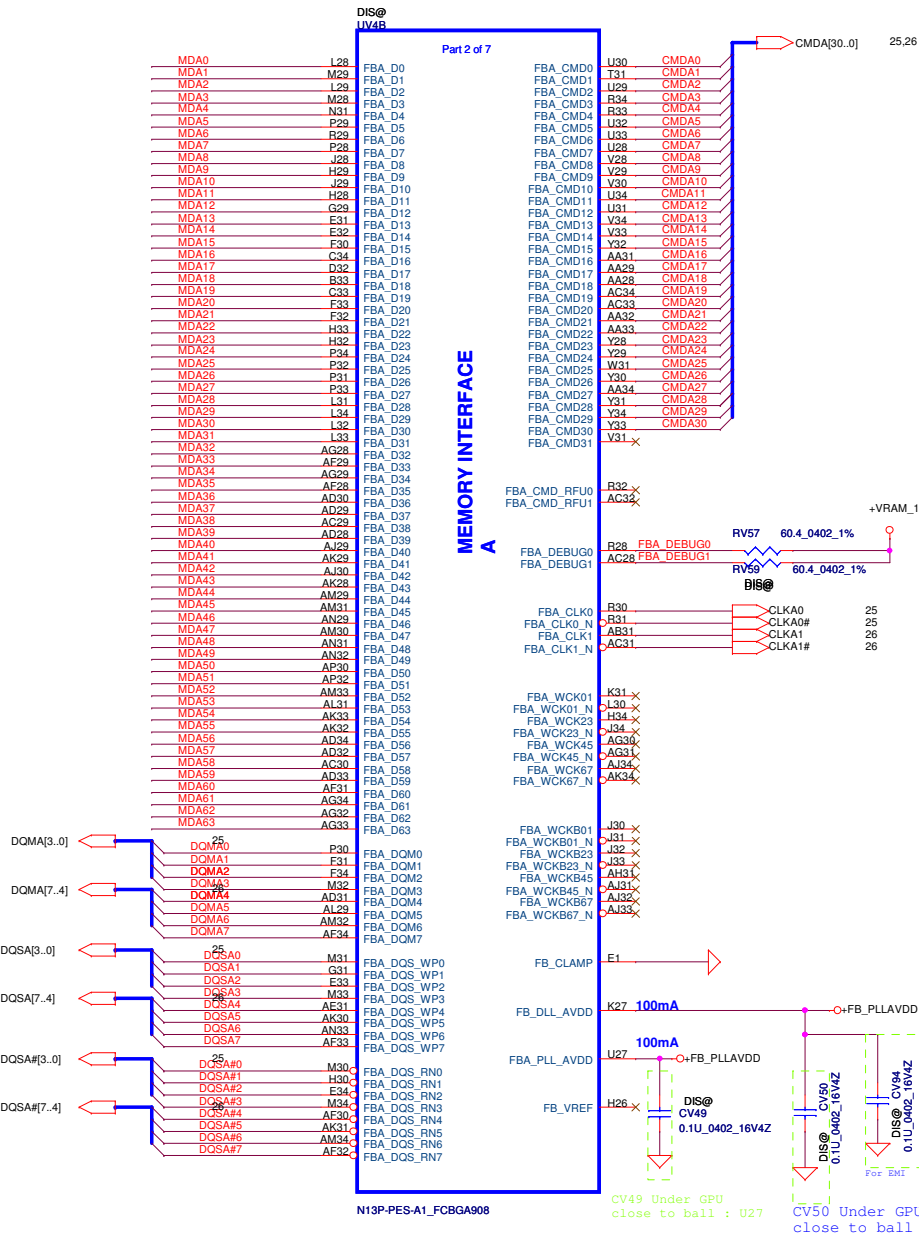
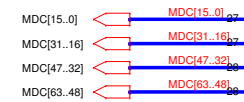
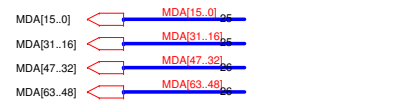


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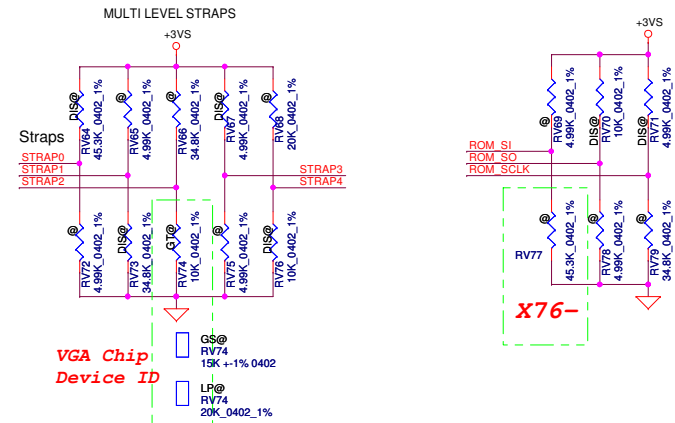


GPIO	I/O	USAGE
GPIO0	O	GPU Core VID4
GPIO1	O	GPU Core VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU Core VID1
GPIO6	O	GPU Core VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU Core VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU Core VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

# VRAM Interface

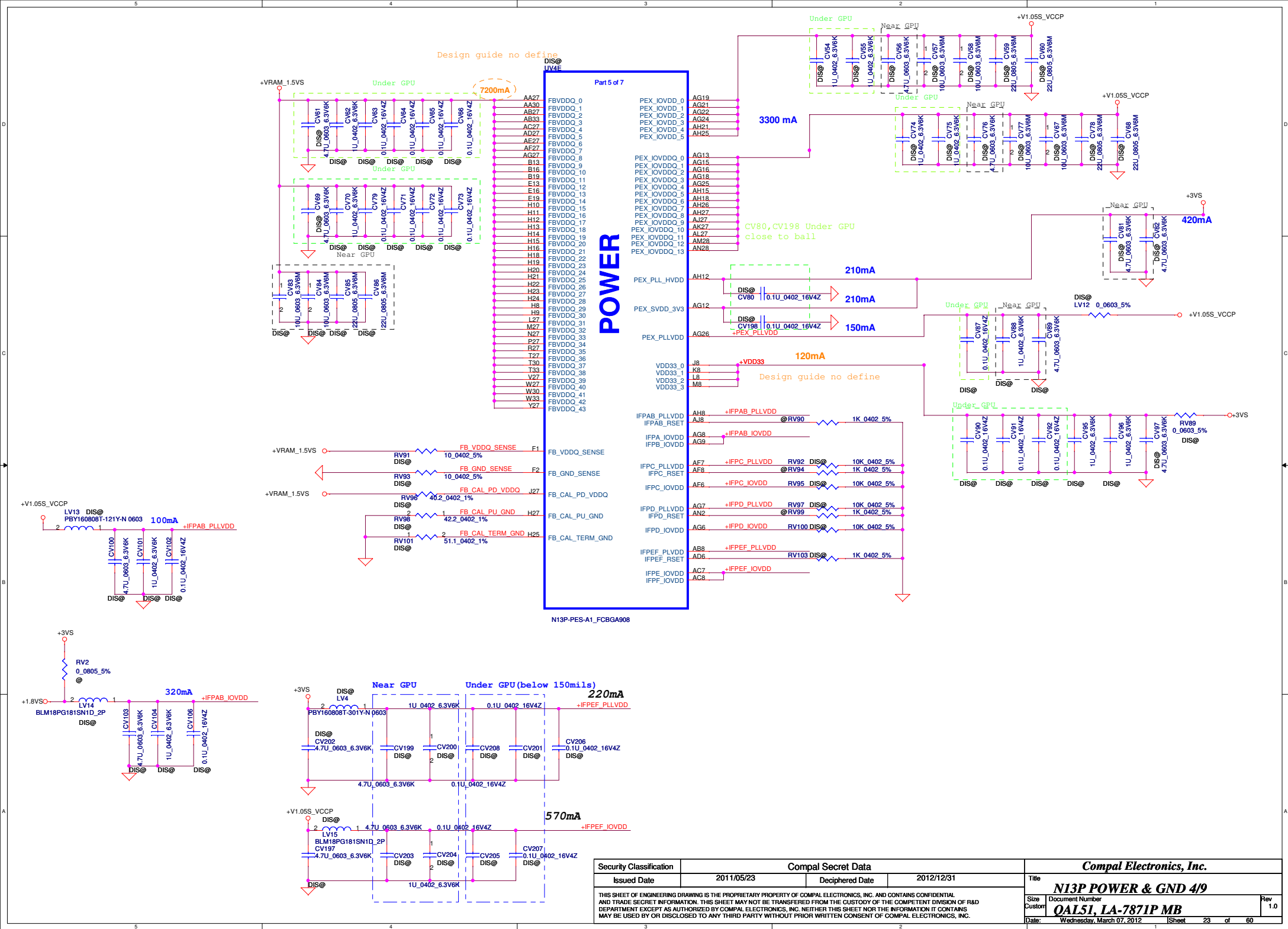


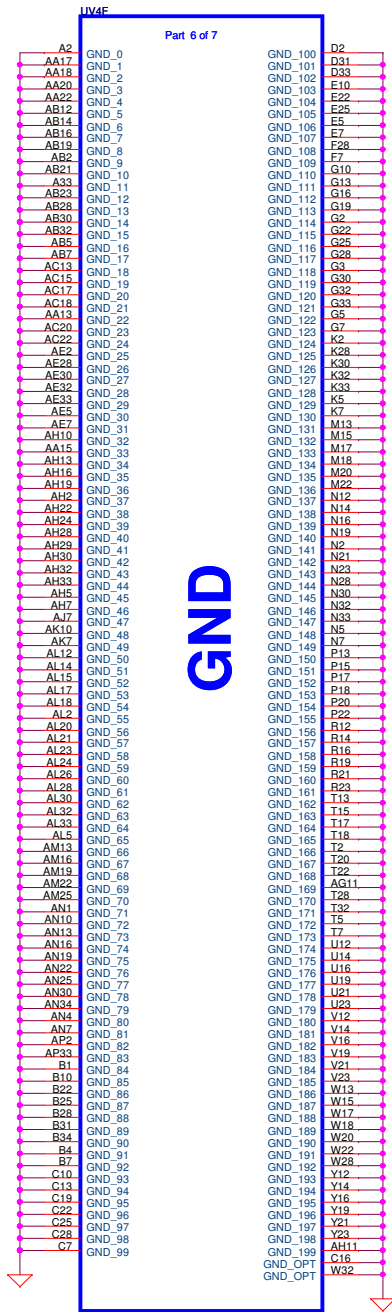
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GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 20K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003Y000	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 35K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 35K	RV74 PD 15K	RV67 PU 5K	RV76 PD 10K	RV77 PD 45K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K
N13P-GT	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 20K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003Y000	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 35K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 35K	RV74 PD 10K	RV67 PU 5K	RV76 PD 10K	RV77 PD 45K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K
N13P-LP	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS00	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 20K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Hynix SA00003Y000	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 35K	RV70 PU 10K	RV71 PU 5K
	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q00	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 45K	RV70 PU 10K	RV71 PU 5K
	900 MHz	64M* 16* 8 1GB	Hynix SA000041S20	RV64 PU 45K	RV73 PD 35K	RV74 PD 20K	RV67 PU 5K	RV76 PD 10K	RV77 PD 15K	RV70 PU 10K	RV71 PU 5K

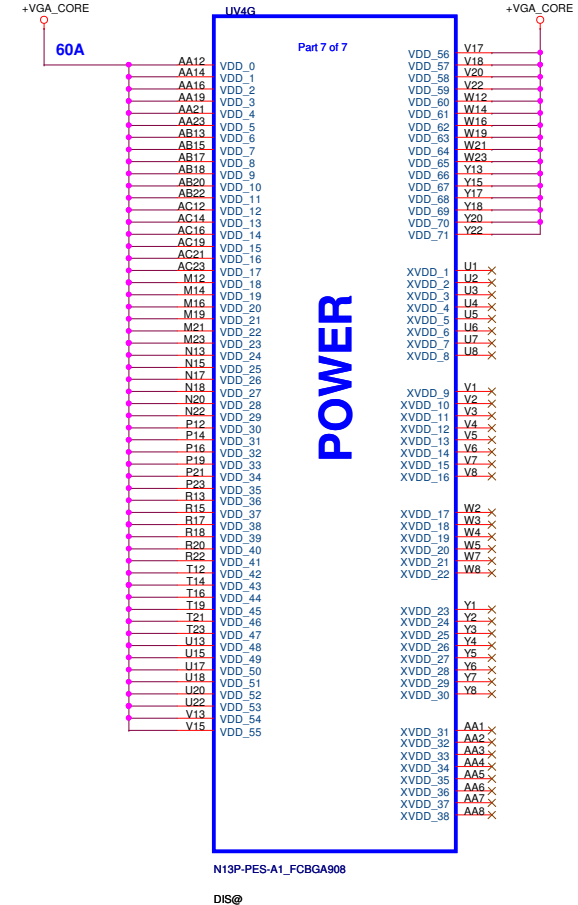






N13P-PES-A1\_FCBGA908

DIS@



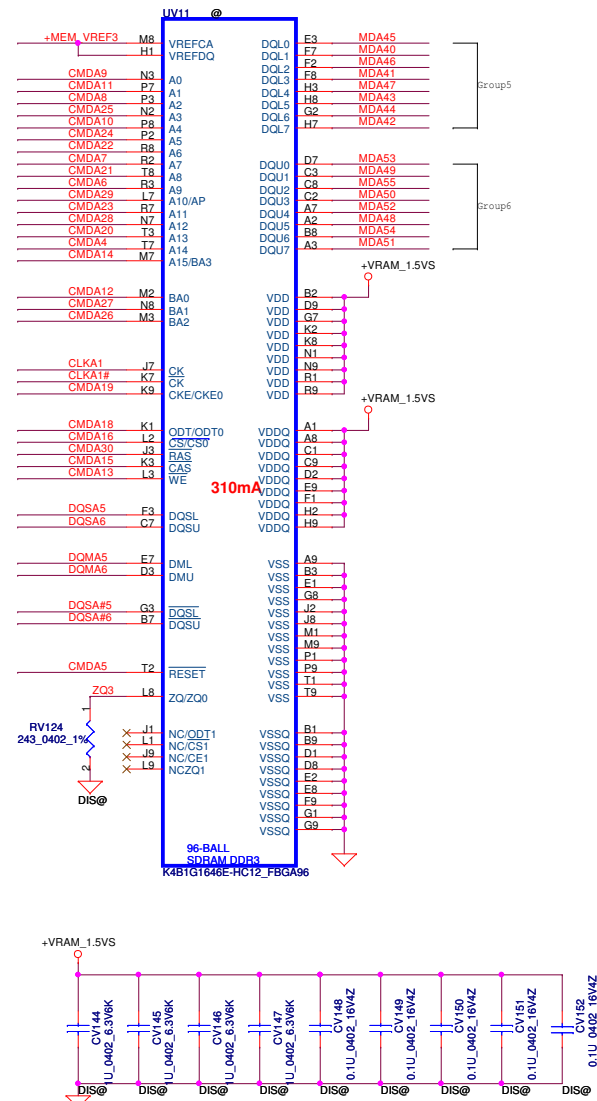
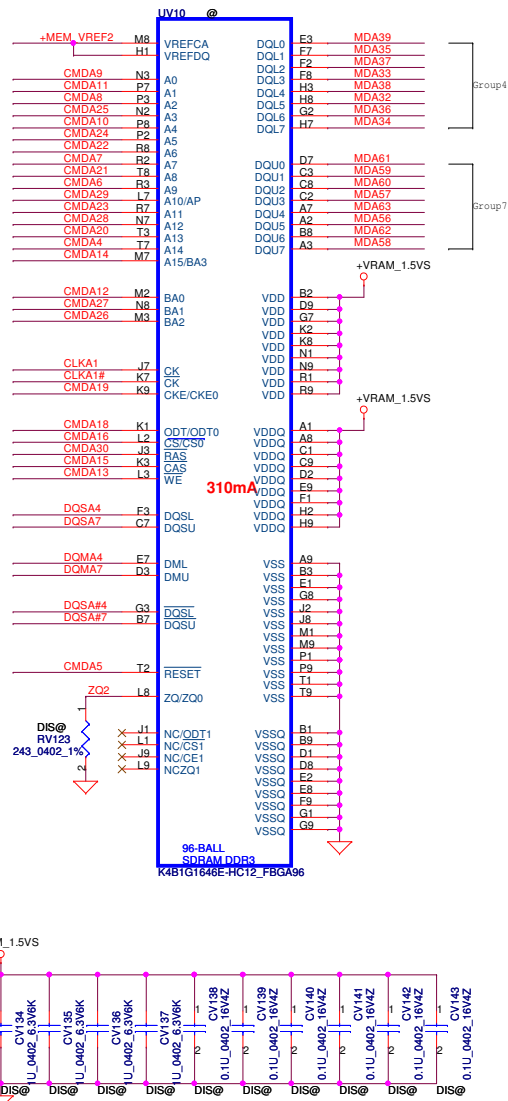
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Issued Date		2011/05/23		Deciphered Date		2012/12/31		Title		N13P POWER & GND 5/9	
Size		Custom		Document Number		QAL51, LA-7871P MB		Rev		1.0	
Date:		Wednesday, March 07, 2012		Sheet		24		of		60	

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64Mx16 DDR3 \*8==>1GB  
128Mx16 DDR3 \*8==>2GB

**128Mx16 DDR3 \*8==>2GB**



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

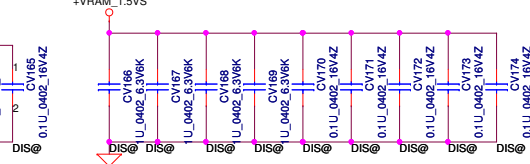
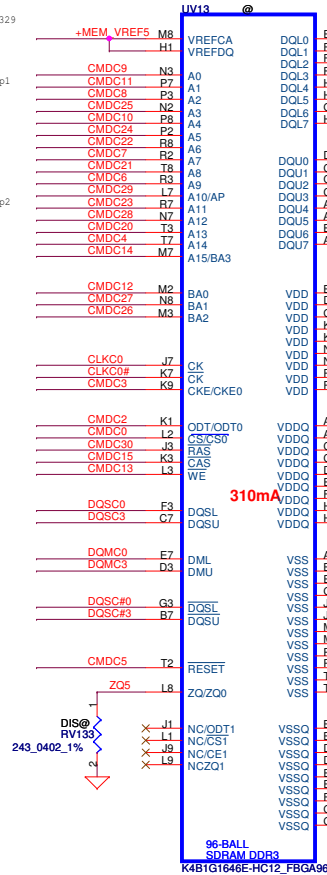
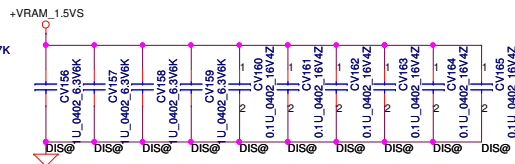
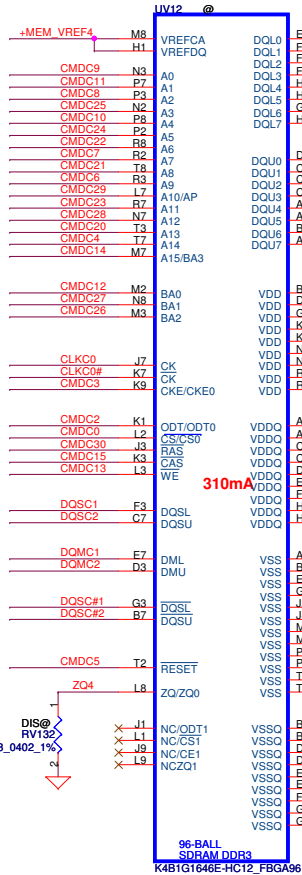
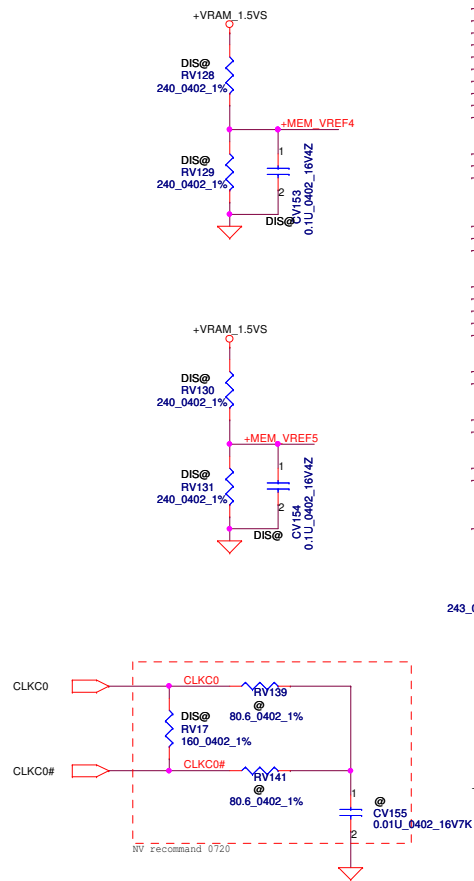
LOW HIGH

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

128Mx16 DDR3 \*8==>2GB

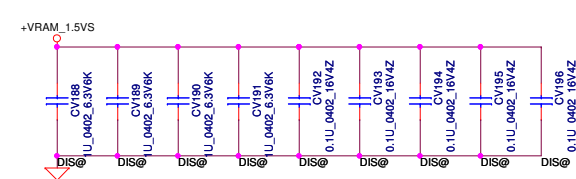
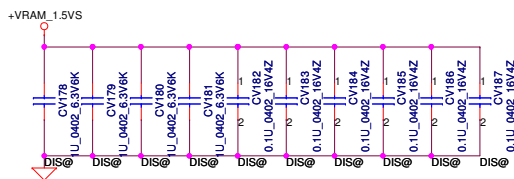
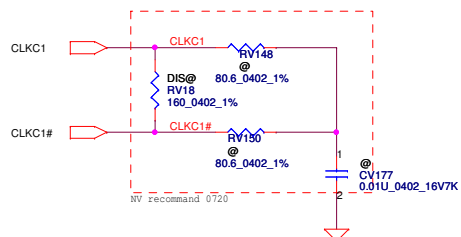
21,28 DQSC[7..0] DQSC[7..0]  
21,28 DQSC# [7..0] DQSC# [7..0]  
DOMC[7..0] DOMC[7..0]  
MDC[63..0] MDC[63..0]  
CMDC[30..0] CMDC[30..0]



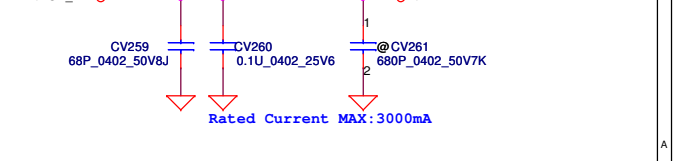
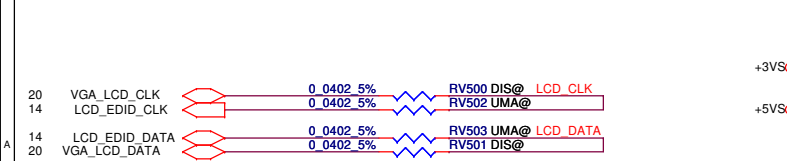
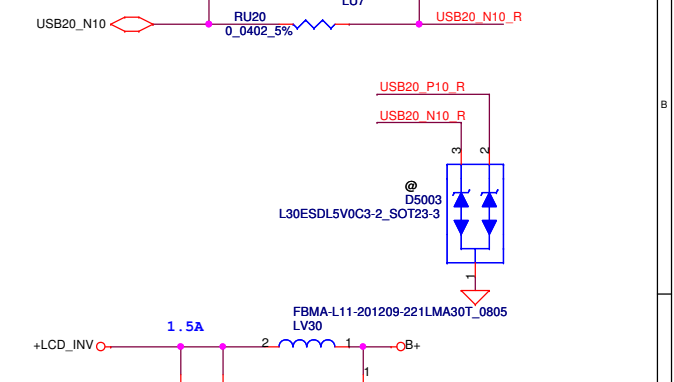
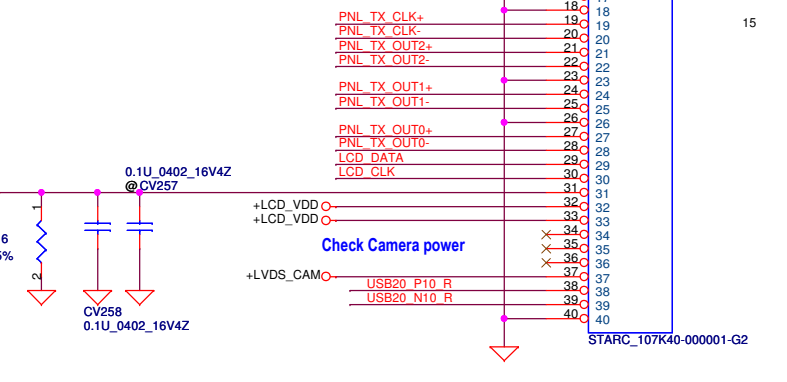
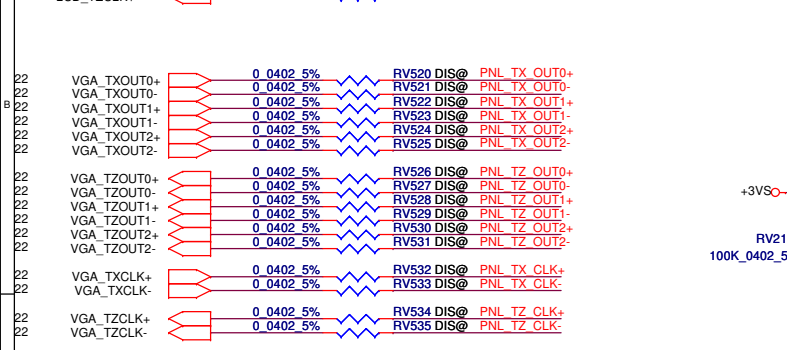
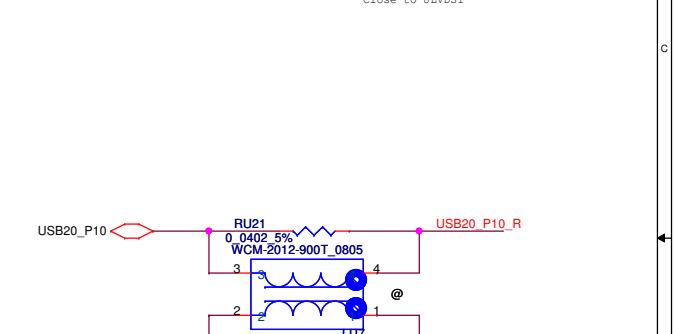
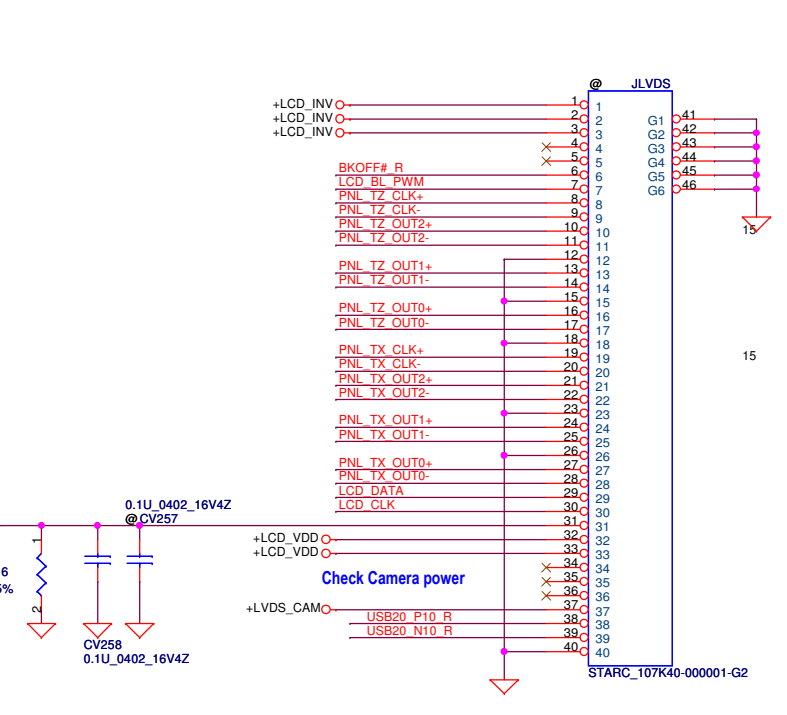
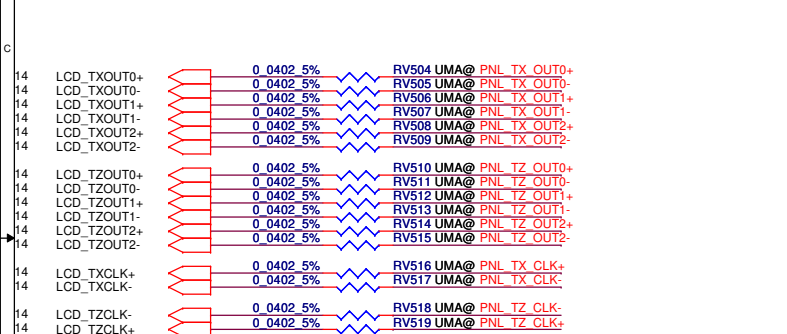
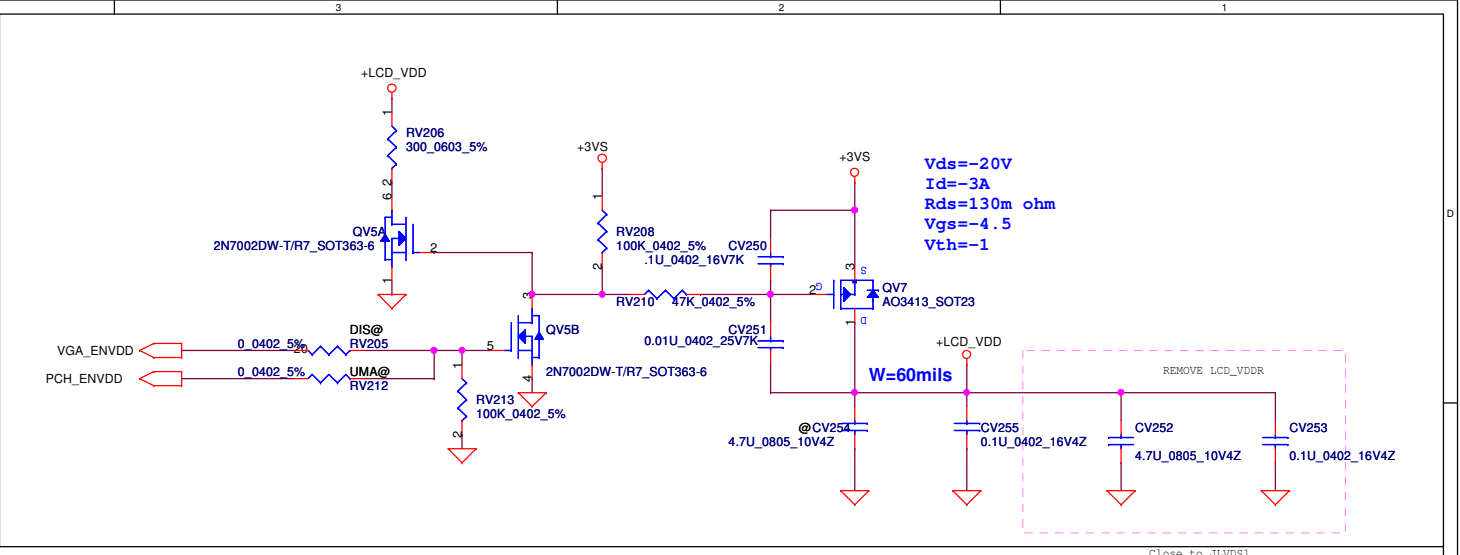
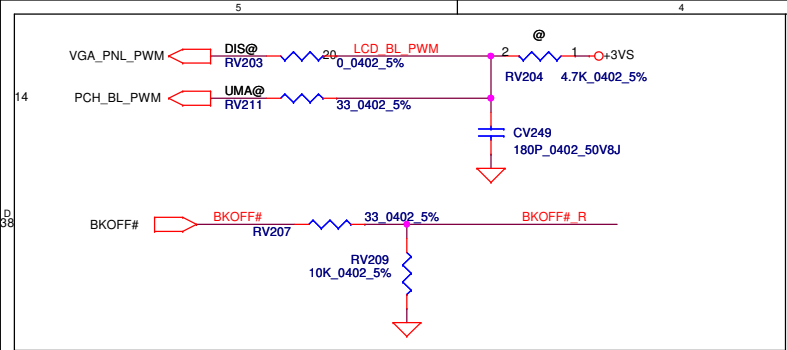
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CkEx	10k
	RST	10k
	CS*	No Termination

**128Mx16 DDR3 \*8==>2GB**

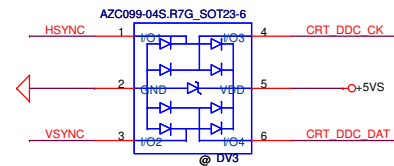
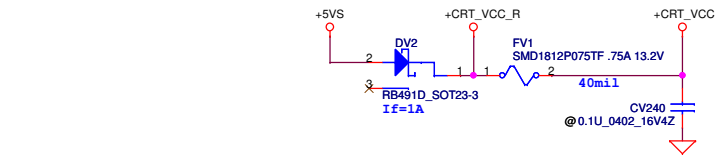
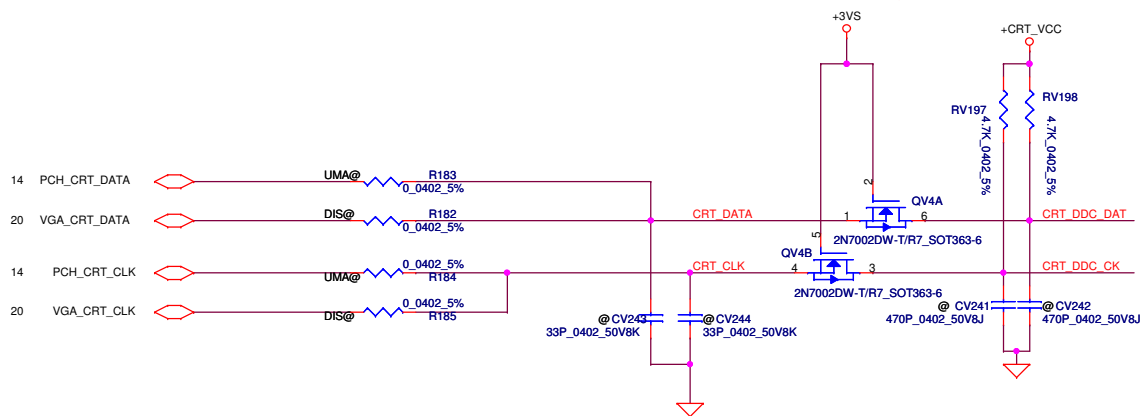
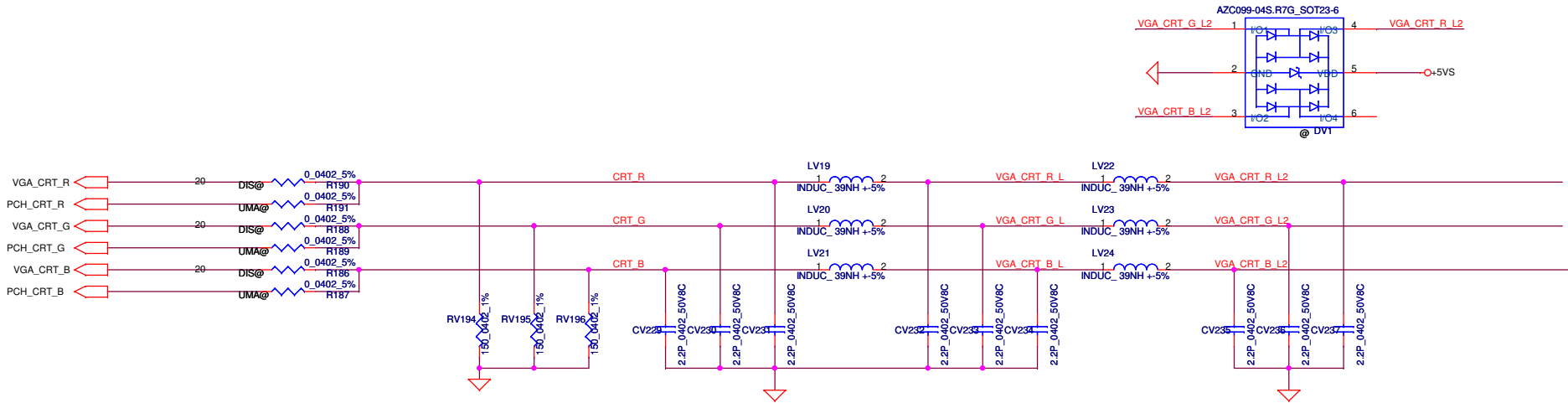


LOW HIGH

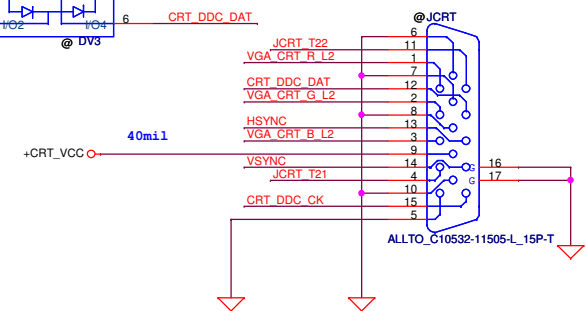
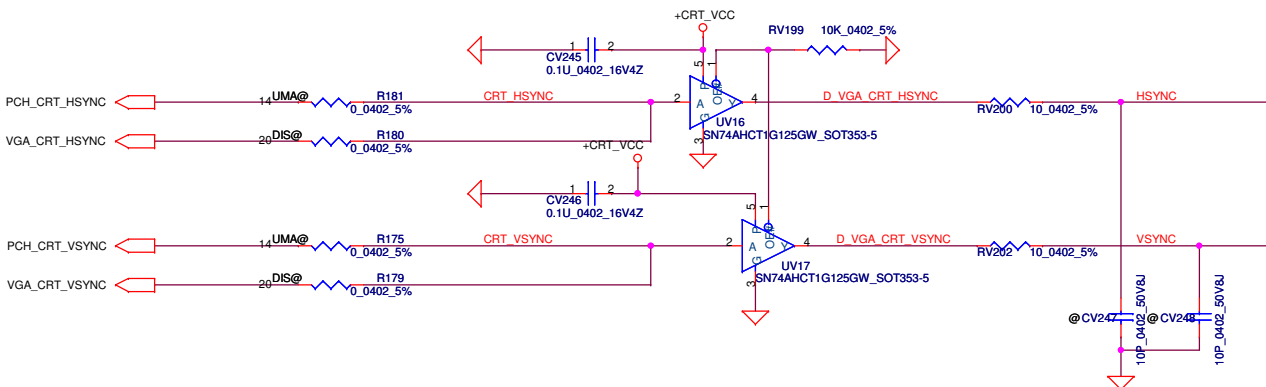


## LCD/PANEL BD. Conn.

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Size		Document Number		Rev	
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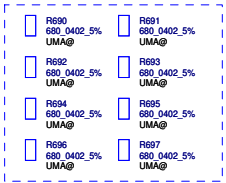
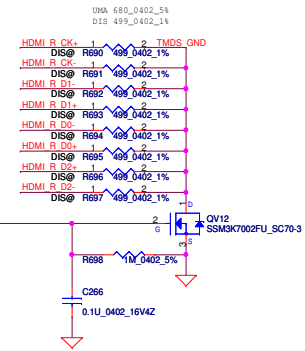
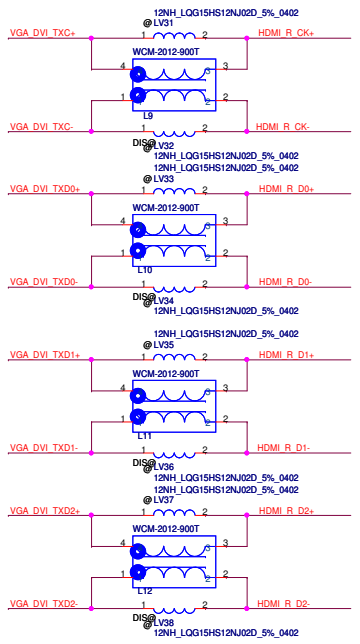
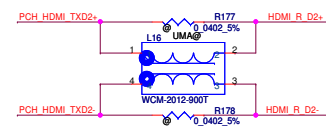
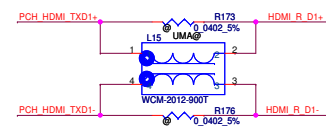
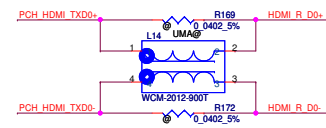
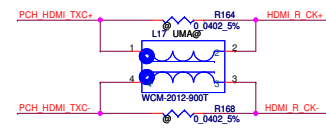
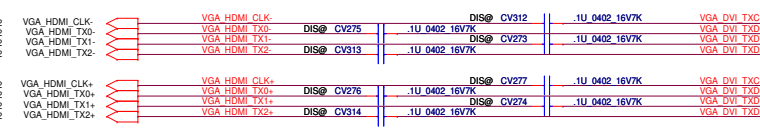
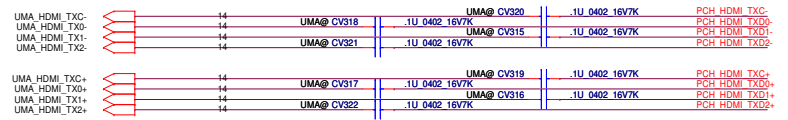
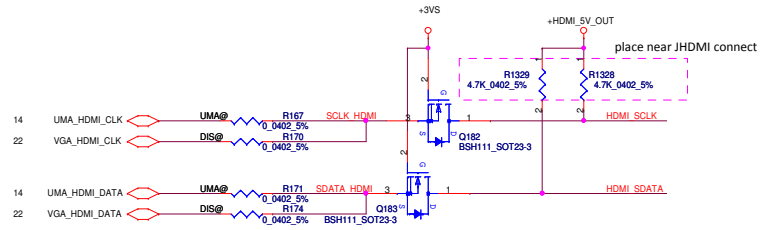
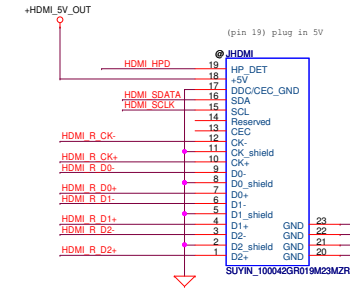
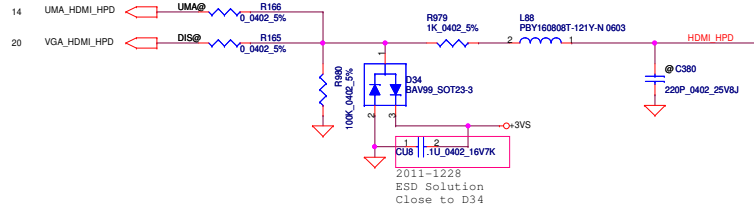
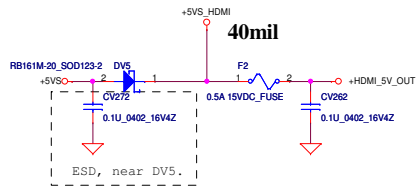
## CRT CONNECTOR



Close to CRT Connector

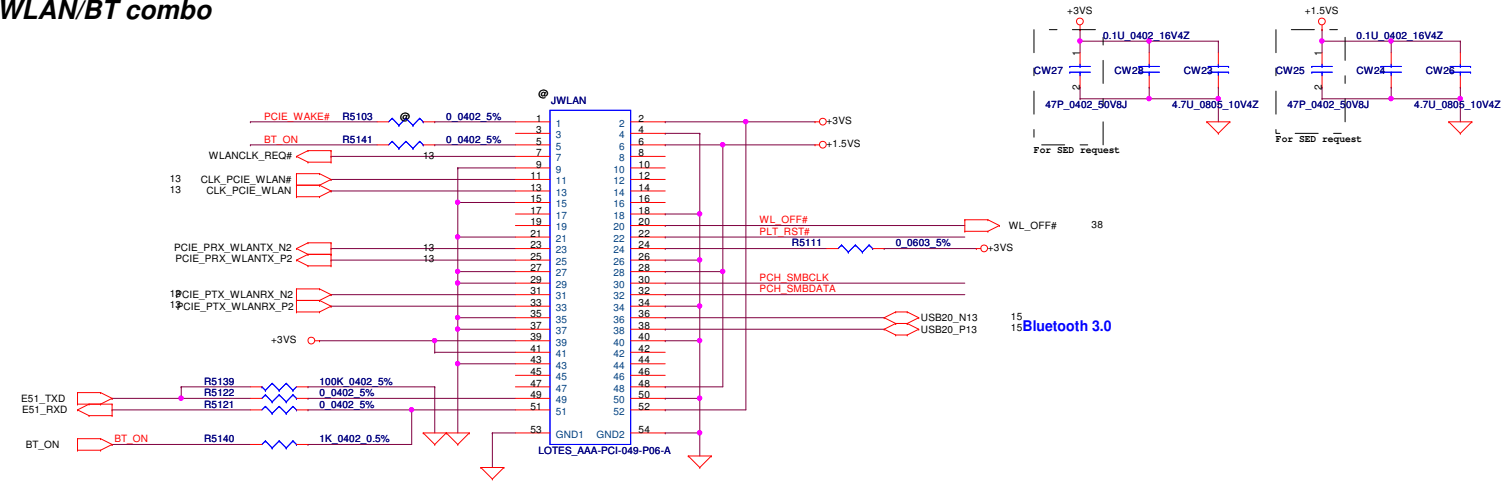
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								1.0			
								Date			
								Wednesday, March 07, 2012			
								Sheet			
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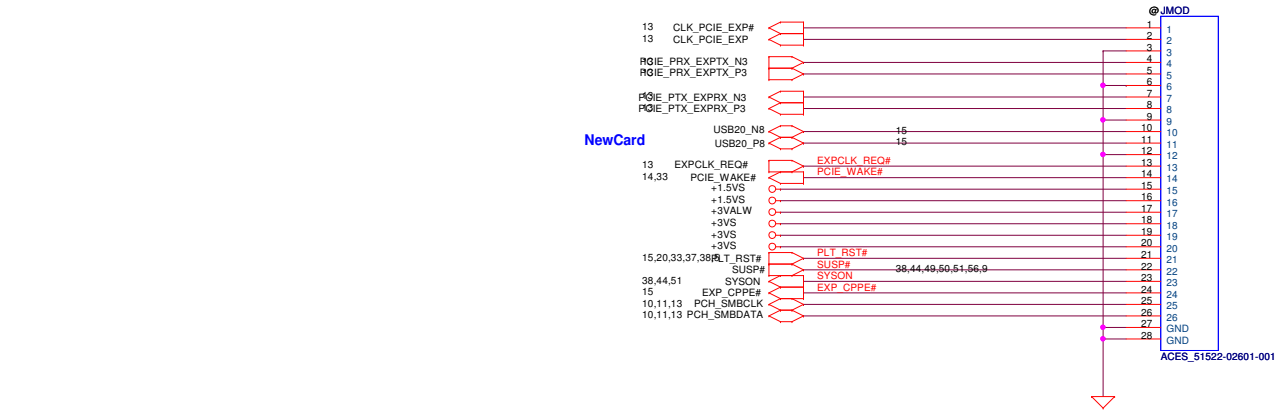


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Document Number		QAL51, LA-7871P MB		Size	
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WLAN/BT combo

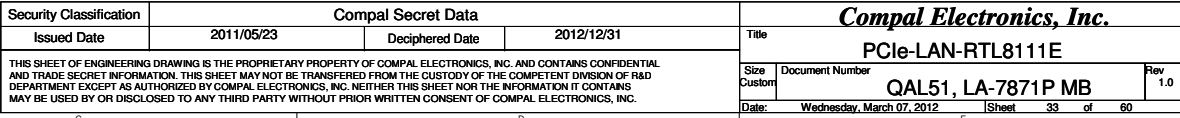


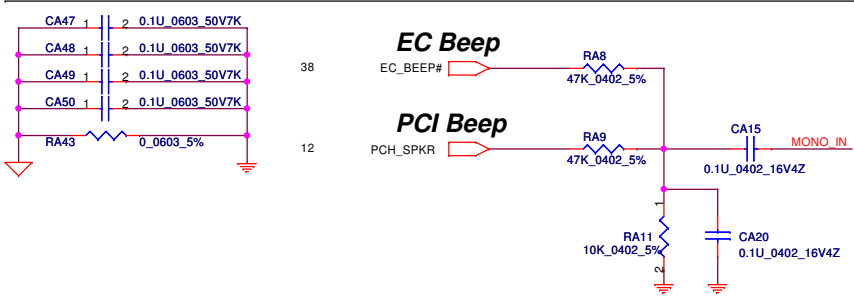
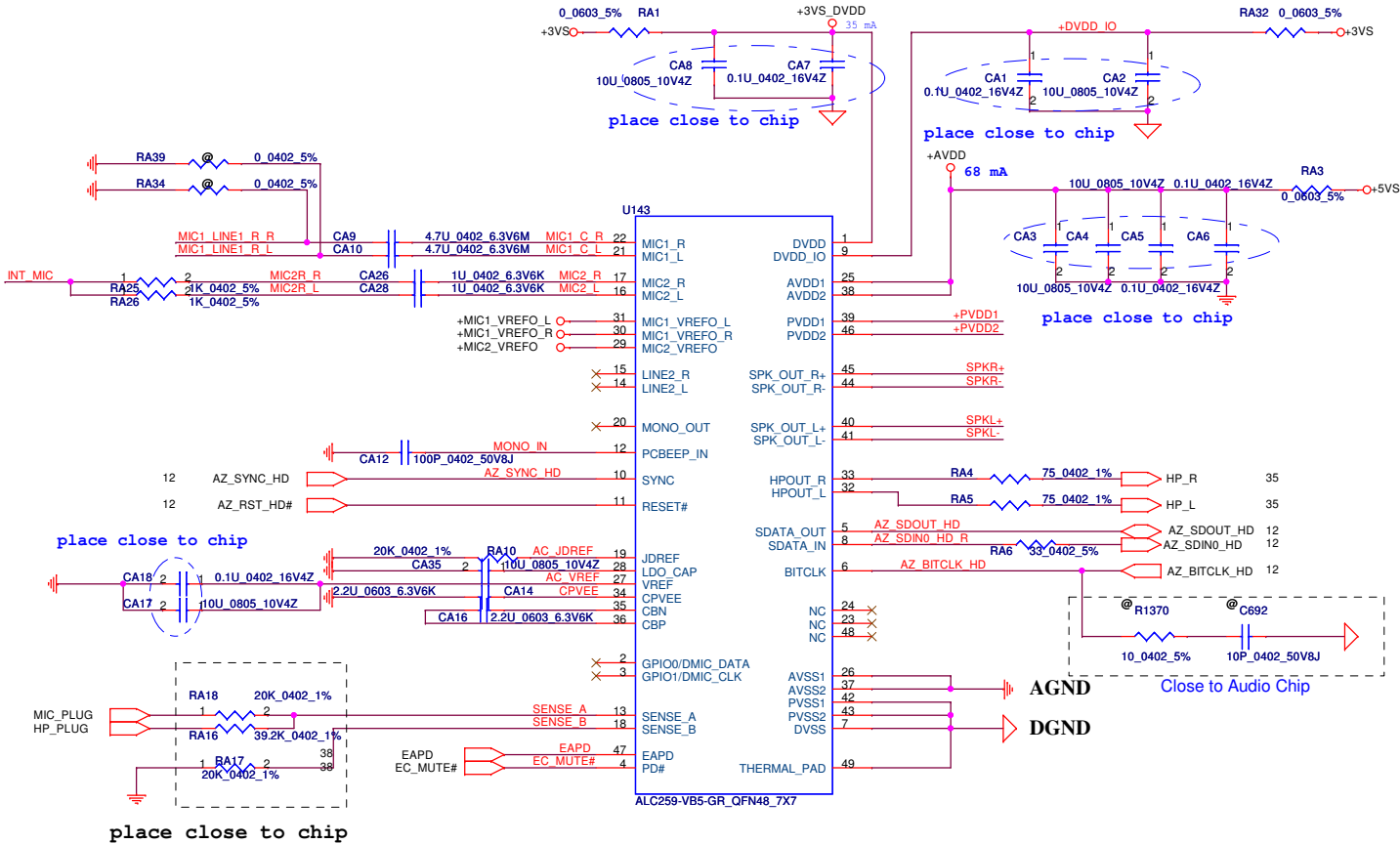
NewCard & Smart Card



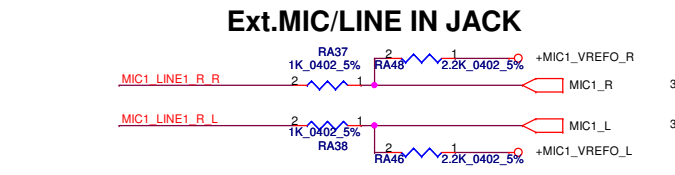
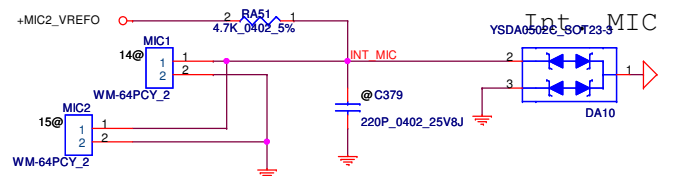
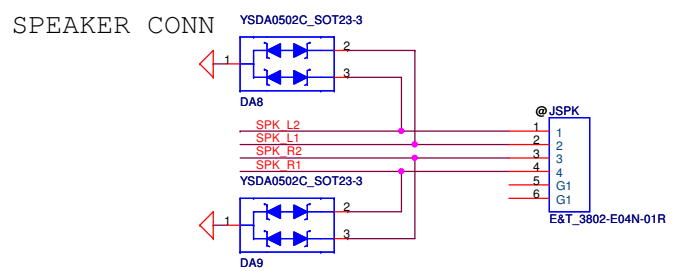
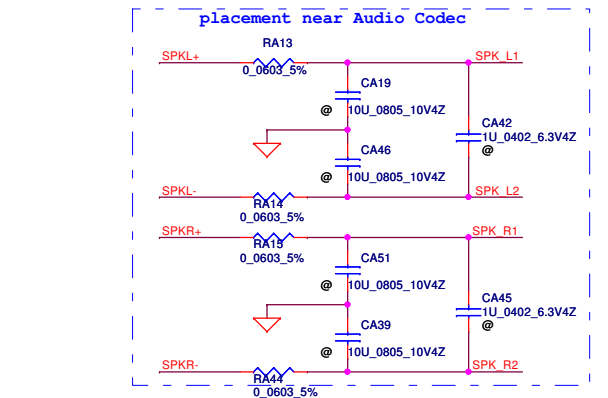
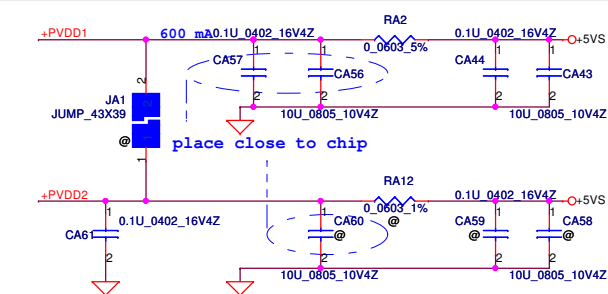
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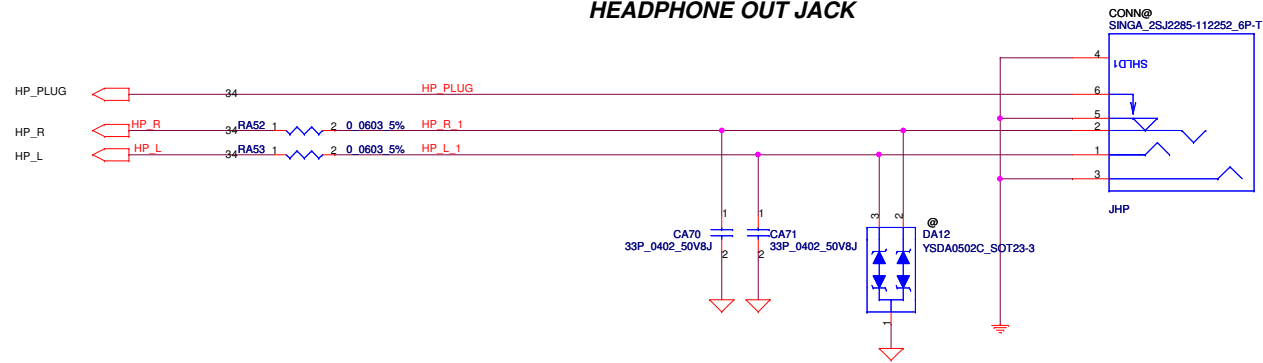


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
SENSE B	20K	PORT-F (PIN 16, 17)	Int. MIC

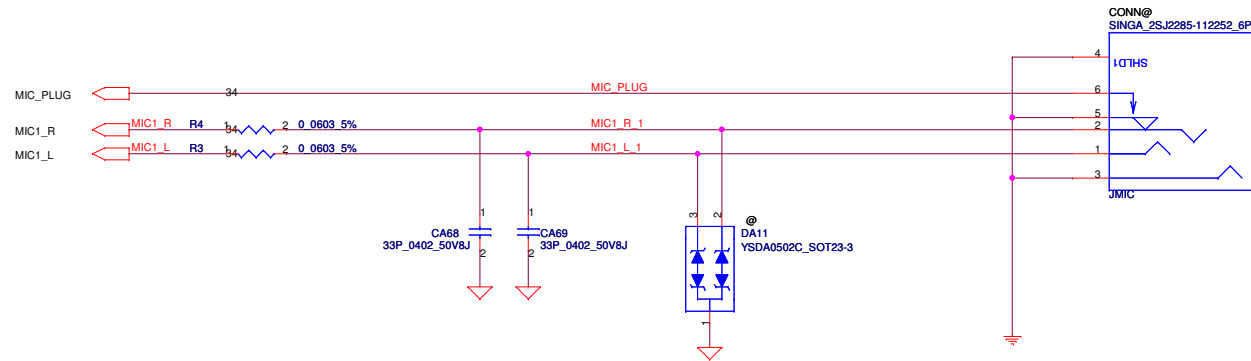


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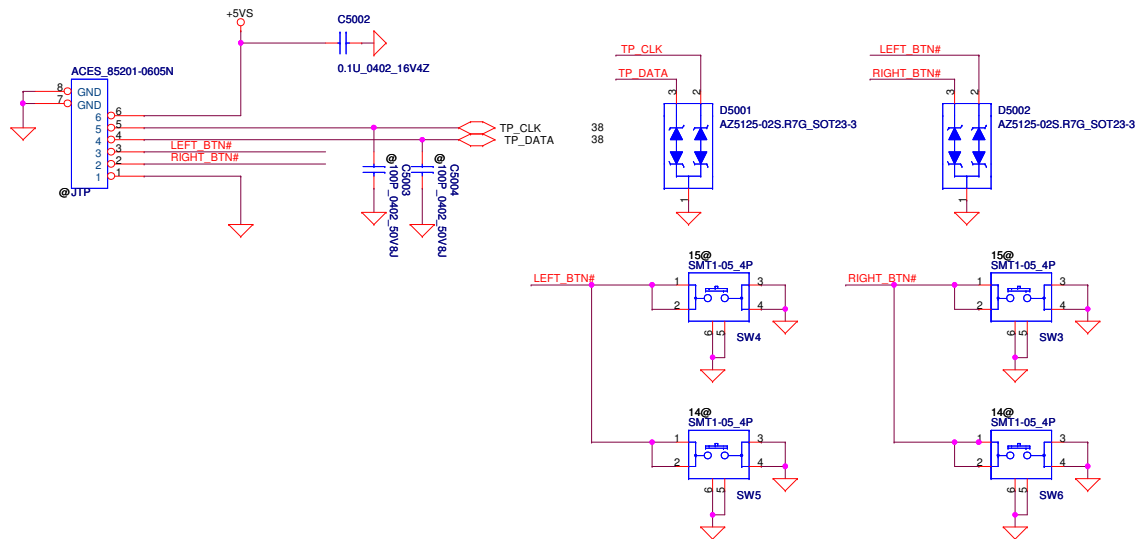
## HEADPHONE OUT JACK



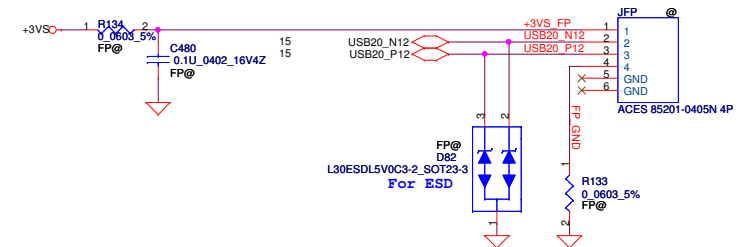
## MICROPHONE IN JACK



## Touch/B Connector

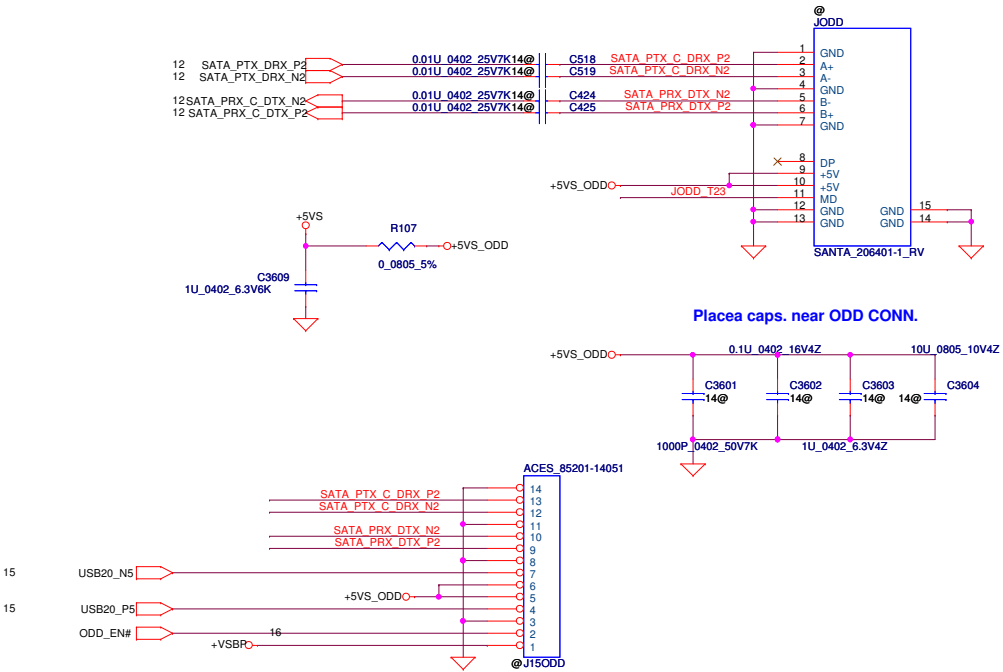


## Finger Printer Connector

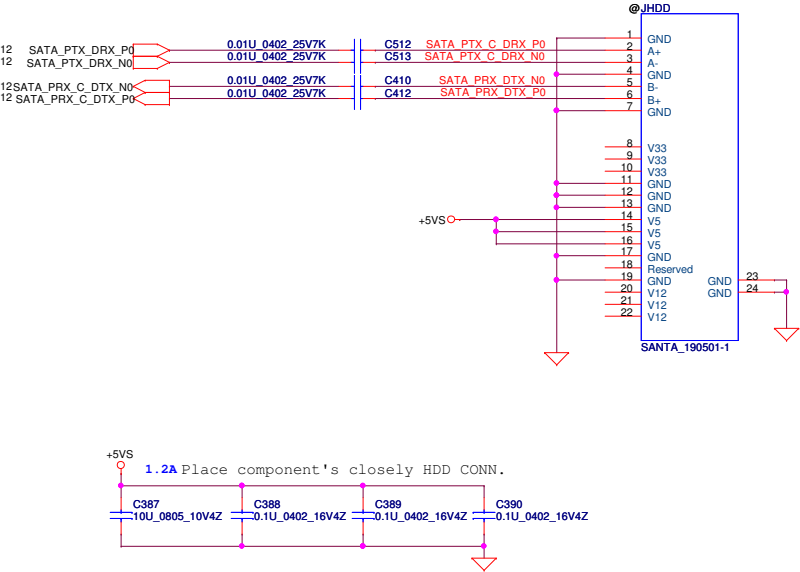


Title			
Card Reader RTSS129			
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SATA ODD Conn.

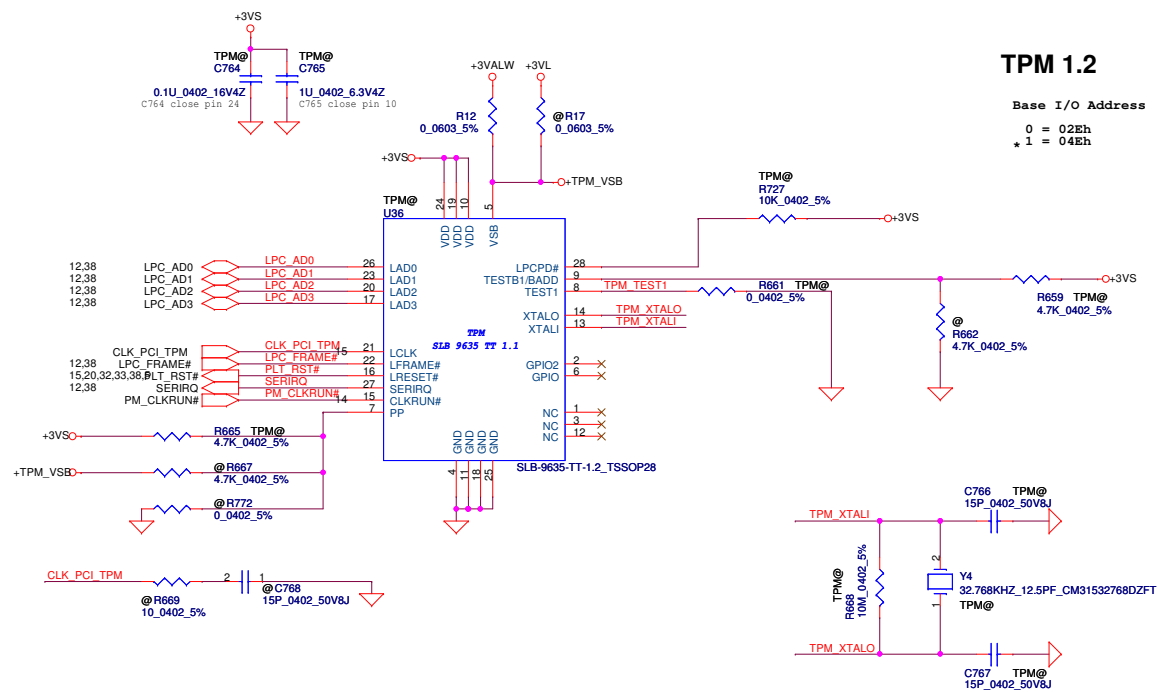


SATA HDD Conn.

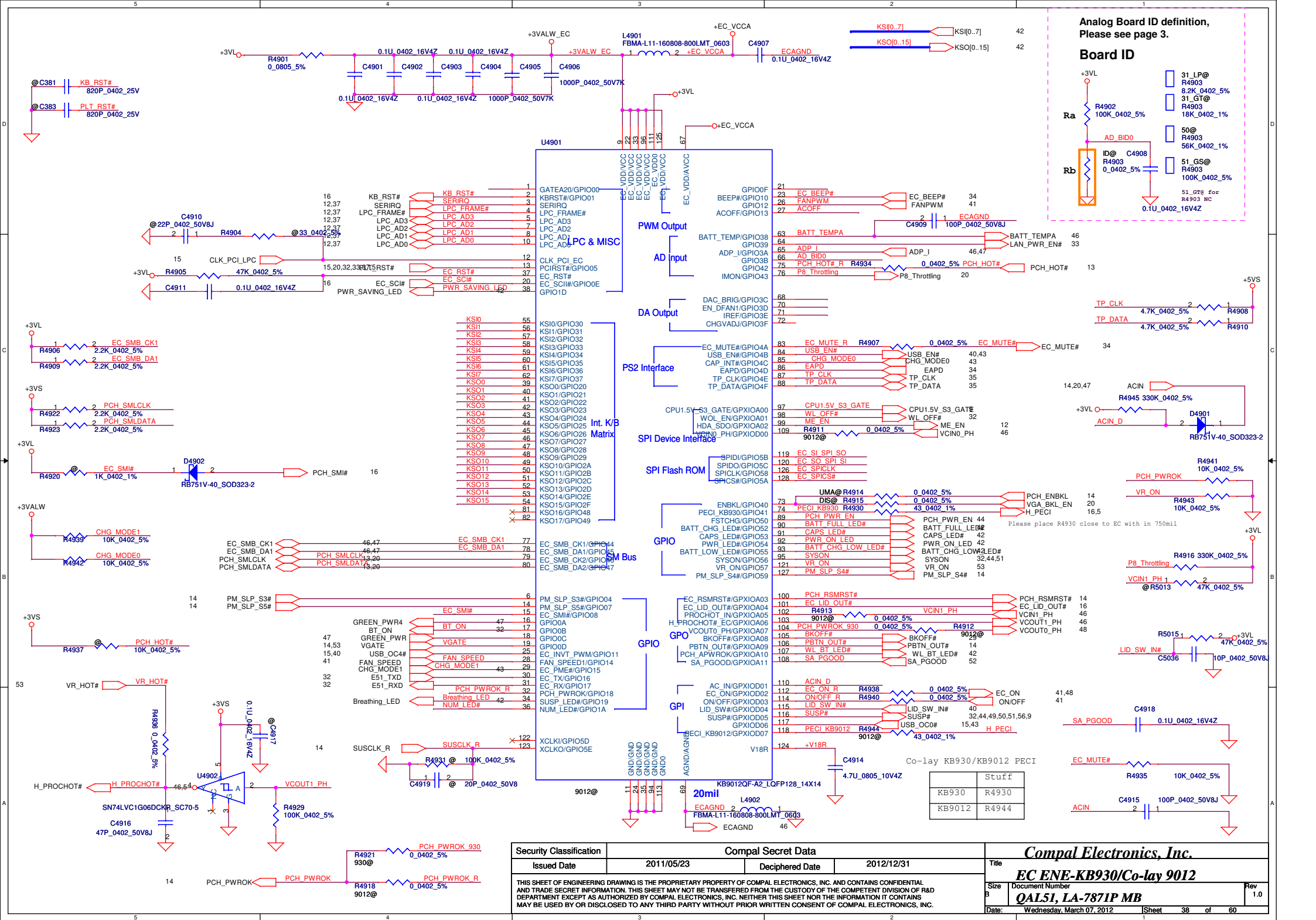


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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	
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Size	Custom	Document Number	QALS1, LA-7871P MB	Rev	1.0
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SPI ROM For Basic ME ROM size  
(w/o Braidwood & system BIOS):  
4MByte

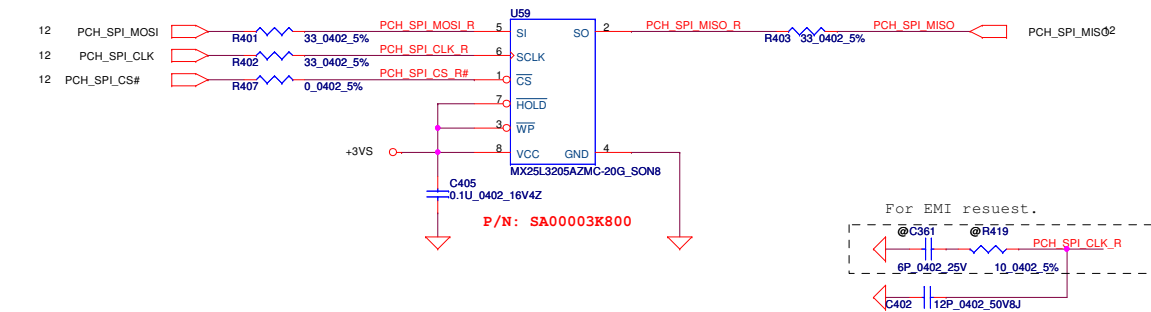


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Issued Date	2011/05/23	Deciphered Date	2012/12/31	TPM	
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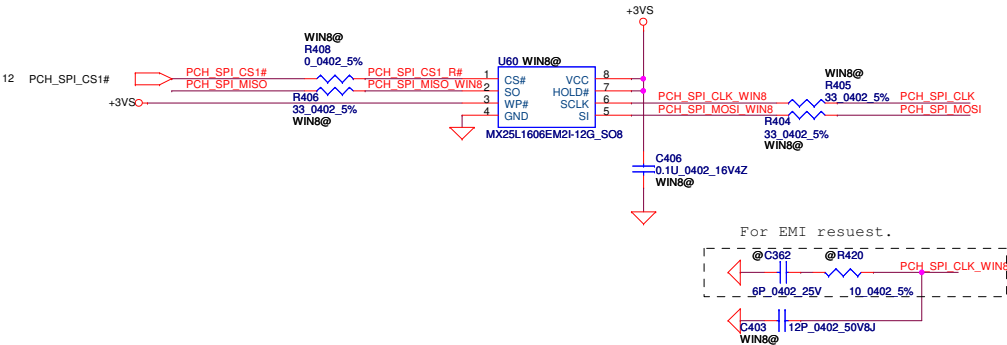


BIOS Bus switch  
SPI ROM For Basic ME ROM size  
4MByte

BIOS SPI Flash (4MByte\*1)



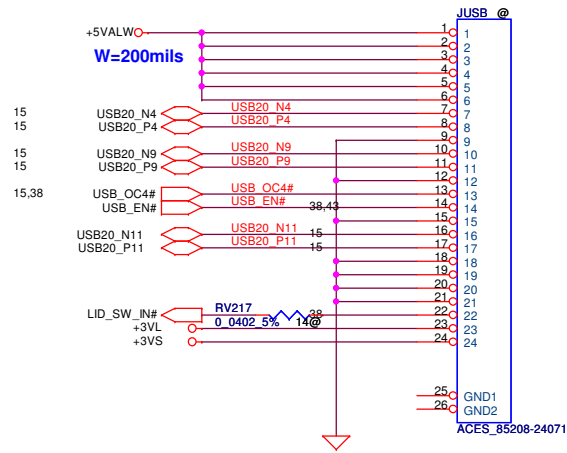
BIOS SPI Flash (2MByte\*1) For Win8



USB + Audio SB

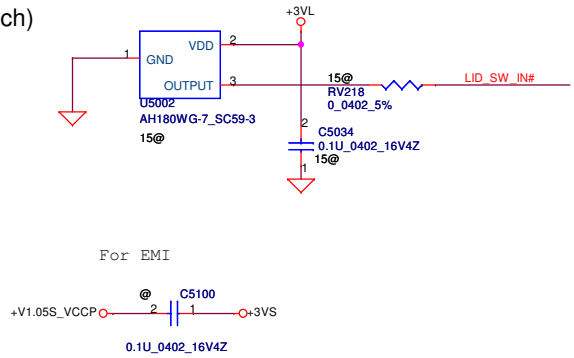
HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK



Lid Switch

(Hall Effect Switch)

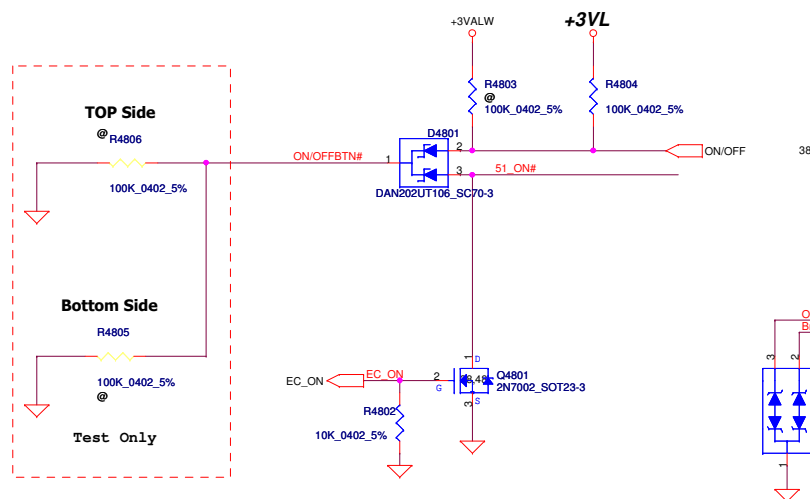


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	
				Function Board	
				Size	Document Number
				QAL51, LA-7871P MB	
				Date:	Wednesday, March 07, 2012
				Sheet	40 of 60
				Rev	1.0

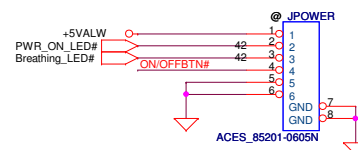


### ***Power Button***

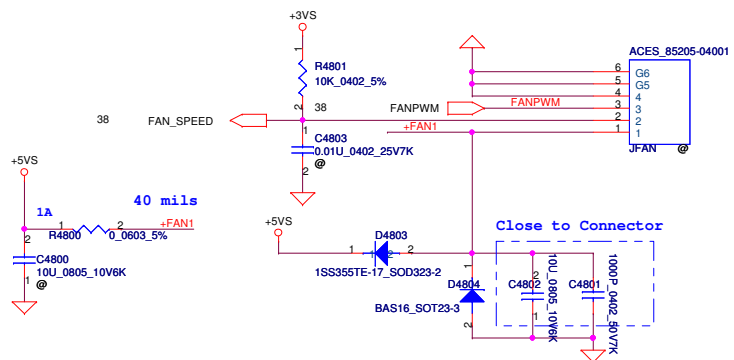
ON/OFF switch



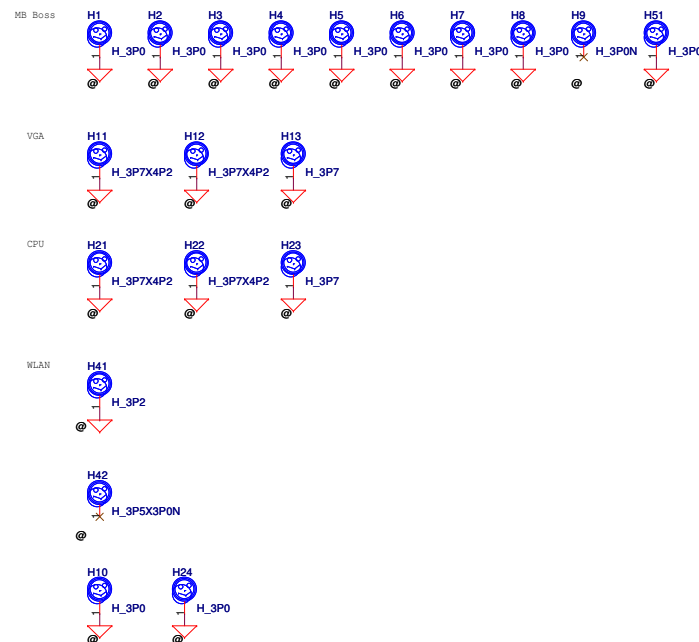
***To POWER/B***



## Fan Control Circuit

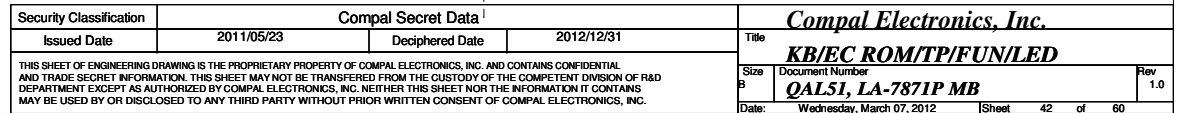


## Screw Hole



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					QAL51, LA-7871P MB	1.
				Date:	Wednesday, March 07, 2012	Sheet 41 of 60

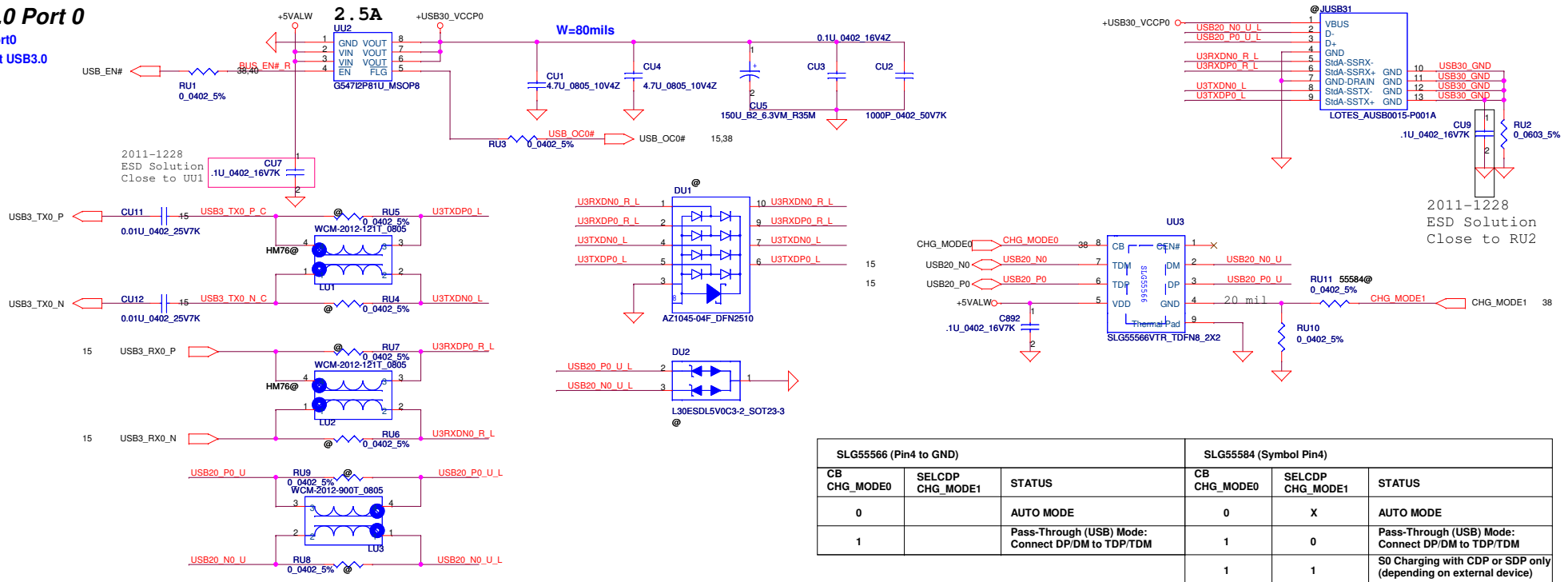
## SATA



## USB3.0 Port 0

USB3.0 Port0

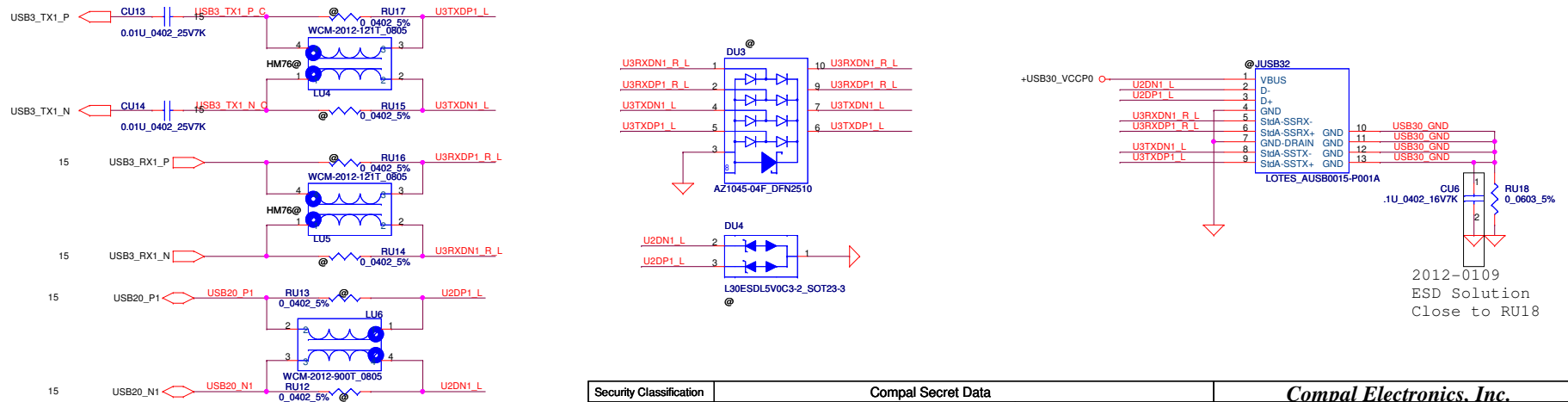
Port 0 : Left USB3.0



## USB3.0 Port 1

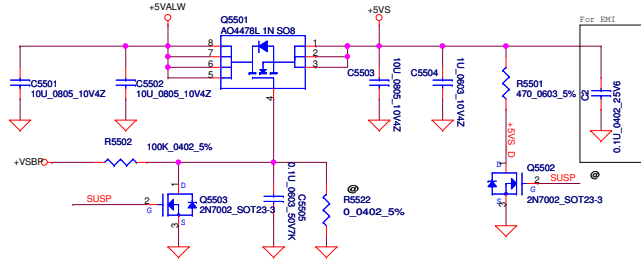
USB3.0 Port1

Port 1 : Left USB3.0 with e-SATA

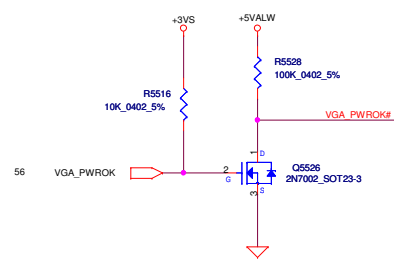
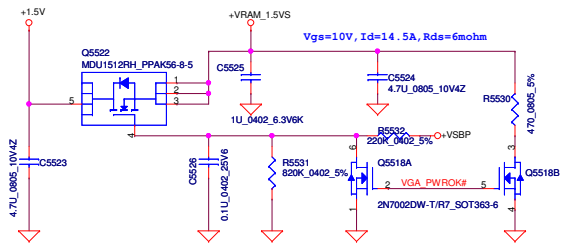


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				Deciphered Date				Power share ENE3810			
				2012/12/31				Size			
								Customer			
								QAL51, LA-781P MB			
								Date			
								Wednesday, March 07, 2012			
								Sheet			
								43 of 60			
								Rev			
								1.0			

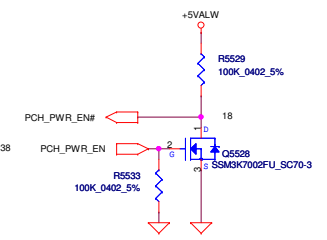
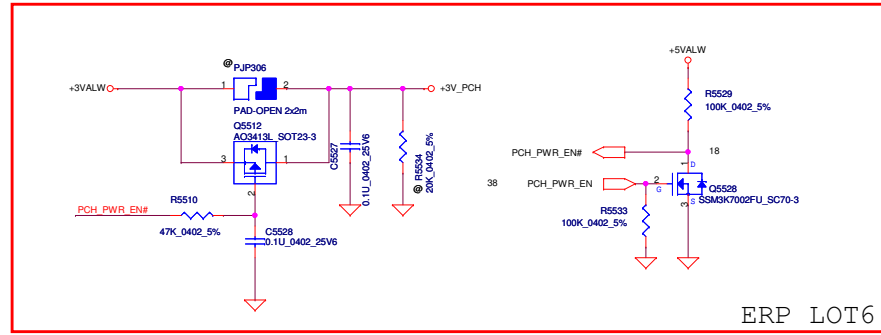
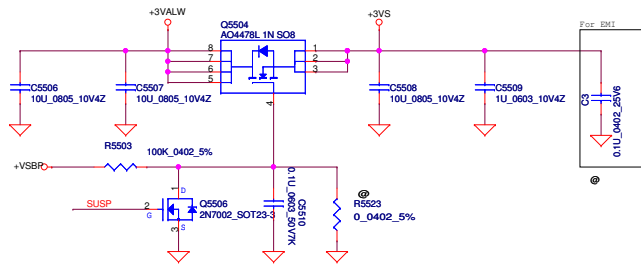
# +5VALW to +5VS



# +1.5V to +VRAM\_1.5VS



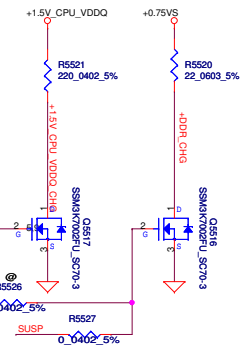
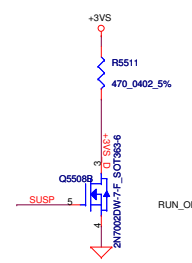
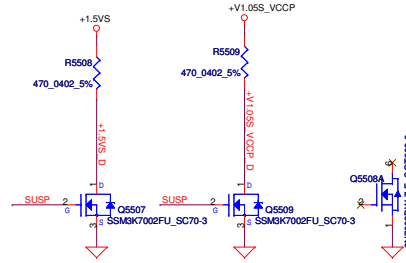
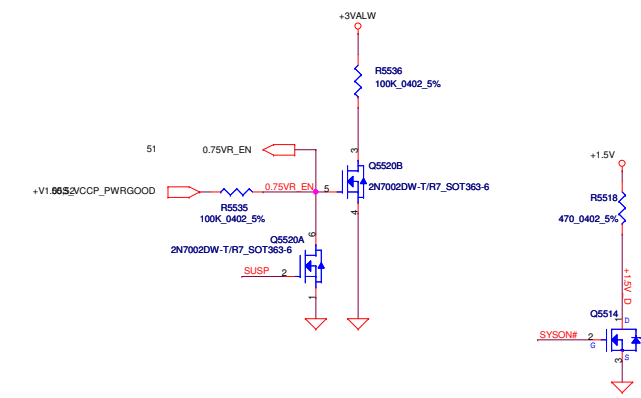
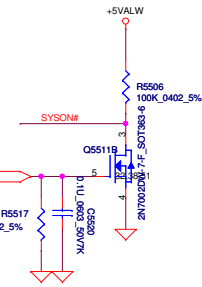
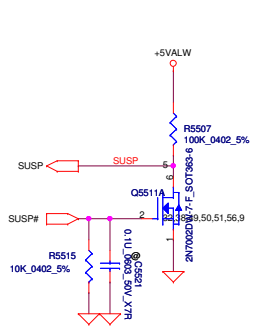
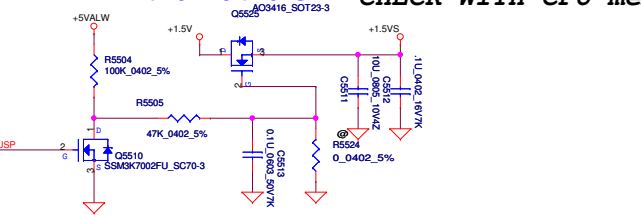
# +3VALW to +3VS



ERP LOT6

# +1.5V To +1.5VS

CHECK WITH CPU memory power



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Date: Wednesday, March 07, 2012				Rev 1.0